Tunneling switching mechanism in non-semiconductor materials

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Abstract

The era of silicon, which can no longer adhere to Moore's Law, is coming to a close. The exponential increase in data due to the development of artificial intelligence (AI) has not been matched by a corresponding increase in the speed of components required for data processing. To overcome these limitations, research is currently underway on switching devices that utilize various 2D materials and switching mechanisms, as well as doping for improved operational speed. One such approach is the metal-insulator-metal (MIM) structure using the tunneling mechanism, which offers many advantages for high-speed operation but suffers from inefficient switching behavior. Researchers are exploring ways to enhance switching efficiency through work function differences [1], geometrical asymmetry [2], and heterojunction tunneling barriers [3], but significant results have yet to be demonstrated.
To address this issue, we propose a novel approach that employs geometric asymmetry and a floating electrode to improve switching behavior. Our proposed transistor features a vertical channel and lateral gate structure for controlling step tunneling by the floating electrode, allowing for high-speed operation and high-efficiency switching concurrently. Compared to conventional CMOS transistors, our transistor exhibited an extremely low leakage current and an extremely low capacitance, thanks to its structural advantages.
Overall, this novel approach has the potential to enhance the performance of conventional FETs and contribute to the development of low-power consumption devices and high-speed electrical systems.

References

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[3] Alimardani, N. et al., Appl. Phys. Lett., 102 (2013) 143501

Figures

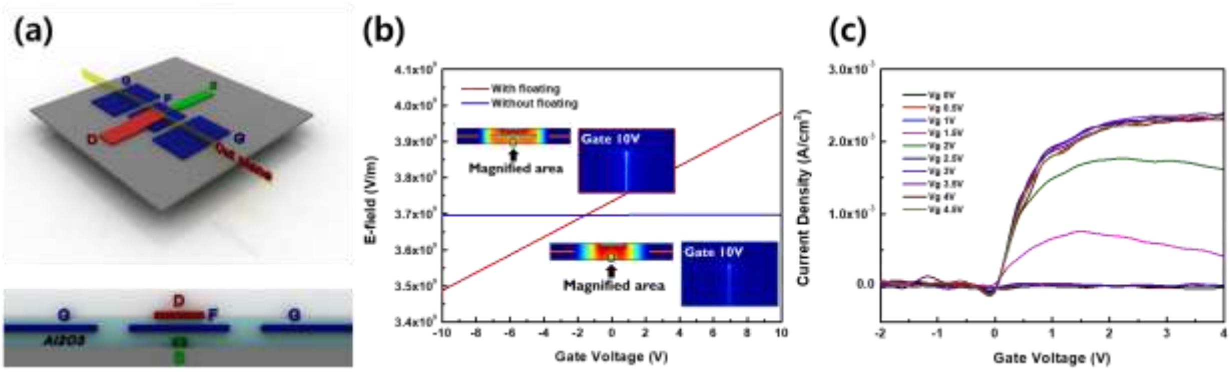

Figure 1: Tunneling switching device by controlling floating electrode (a) schematic lustration (b) the effect of a floating electrode to tunnelling switching behavior (c) the electrical characteristics of tunnelling device with floating electrode