Best Combination of Selector Technology and Memory Element to Achieve High Density and Low Power Crosspoint Arrays for SCM Applications

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Abstract

In the area of booming in electronic components (smartphones, tablets, pc, smart home gadgets) combined with new applications (AI, Face and Speech recognition) – all generate a huge quantity of data that need to be stored efficiently and accessed fast. A better trade-off compared to what Flash and DRAM can provide is not sufficient to meet power-performance-density-cost requirements. Emerging non-volatile memory (NVM) such as PCM, RRAM, MRAM, FeRAM, can offer good option for Storage Class Memory (SCM) applications considering their speed is in the range of ~ns, their excellent scalability beyond 10nm and low power capability[1,2,3]. To improve the memory density, NVM can be integrated in Crosspoint configuration where word lines (WL) are orthogonal to bit lines (BL) and the memory cell is placed in between the two electrodes. The main issue of this configuration is the presence of leakage or IR drop for half-selected cells with consequent degradation of the memory performance, variation of the electrical response and uncontrol of current and voltage of the cell. A possible solution consists in replacing the memory element with 1 Transistor and 1 Resistor, but the cell is mostly limited to the transistor performance and does not match well with scaling demand. Another option is to implement 1Diode-1R which has unipolar and high thermal budget, unfortunately self-rectifying cells are implemented but not mature enough. 1Selector-1R seems the best option. Selector technology (FAST, OTS, MIEC, VCB...)[4,5] are based on different mechanisms such as barrier engineering, threshold switching or volatile behaviour. The requirements for SCM need the selector to satisfy some parameters such as ON current density of >10MA/cm, very low leakage of pA, high selectivity>1E6, CMOS compatible processing temperature <400°C and scaling proportional to resistance element[2,6,7]. The important task is to find the good match between NVM element and Selector. Many options are presented by different industry players such as OTS+PCM, OTS+OxRAM, OTS+RRAM, Hf-based Selector +MRAM reported in Fig.18. These options show already good performance in Mbit arrays and integrated in advanced 20nm node. The race is still open and researchers have the possibility to optimize 1S1R cell to overcome challenges such as memory wall (beyond Van Neuman - CiM, Hybrid Memory architecture) and integration from planar to vertical 3D structures (with optimized ALD process for scaled devices)[9].

References

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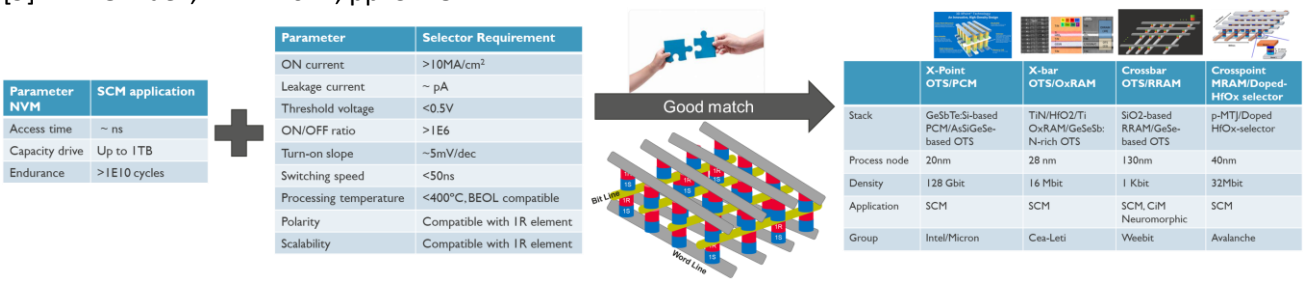

Figure 1: NVM technology and requirements in combination with Selector technology and specifications to achieve best 1S1R Crosspoint architecture towards SCM, ML and Neuromorphic applications [1-9].