Partially reduced graphene/silicon interfaces via electrochemical reduction

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Abstract

The relatively recent progresses in the characterization of true graphene deposits have allowed a much better interpretation of results in the field, also allowing for a comparison between the outcomes of distinct synthetic strategies aimed at partially reduced forms of graphene oxide.[1,2] A notable goal in view of studies and applications of graphene is the obtainment of handy forms of this material, allowing for developments in real conditions. To achieve applications, a large-scale production of high quality graphene sheets in an efficient and effective way is required.[3]
Wafer-scale integration of reduced graphene oxide with H-terminated Si[111] surfaces has been recently accomplished by electrochemical reduction of a thin film of graphene oxide deposited onto Si by drop casting.[4,5] Distinct reduction methods have been assayed and carried out in solution. The resulting interface has been characterized in its surface composition, morphology and electrochemical behavior by X-ray photoelectron spectroscopy, Raman spectroscopy, atomic force microscopy and electrochemical measurements. The results evidence that few-layer graphene deposits on H-Si[111] were obtained after reduction, with a very limited surface oxidation of the Si substrate and a very low oxygen-to-carbon ratio. The described approach is fast, simple, economic, scalable and straightforward, as one reduction cycle is already effective in promoting the establishment of a graphene-Si interface. It avoids thermal treatments at high temperatures, use of aggressive chemicals and the presence of metal contaminants, and enables preservation of Si[111] surface from oxidation. This may favour applications in biomedicine, rapidly growing innumber and importance in the last few years.[6]

References

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