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Continue the transistor scaling with 2D materials: Challenges and Perspective

Internet of things and artificial intelligence demand further transistor performance improvements and device size scaling. In a conventional planar silicon field-effect transistor (FET), the gate controllability becomes weaker when its lateral dimension scales. Hence the transistor body thickness needs to be reduced to ensure efficient electrostatic control from the gate. When the silicon thickness reduces to a few nanometers, the fast mobility decay owing to the scatterings from imperfect silicon surfaces retards the further scaling. New materials with perfect surfaces are therefore needed and 2D semiconducting materials offer a chance to continue the scaling.

Silicon transistor evolution shall be discussed first. Many challenges are ahead for adopting 2D semiconductors as FET channel materials, including (1) selection of 2D materials, (2) reduction of contact resistance, (3) growth of wafer-scale and single-crystalline 2D materials, and (4) Integration of 2D materials to existing microelectronic fabrication processes. In this presentation, we will discuss on these challenges and possible approaches.