# Weight-four parity checks with silicon spin qubits

**Yi-Hsien Wu**[1]
Brennan Undseth[1,*], Nicola Meggiato[1,*], Sam R. Katiraee-Far[1], Larysa Tryputen[2], Sander L. de Snoo[1], Davide Degli Esposti[1], Giordano Scappucci[1], Eliška Greplová[1] and Lieven M. K. Vandersypen[1]

[1]*QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands*
[2]*Netherlands Organization for Applied Scientific Research (TNO), Stieltjesweg 1, 2628 CK Delft, Netherlands*
**These authors contributed equally to this work.*

Y.H.Wu@tudelft.nl

## Abstract

Recent advances in coherent spin shuttling [1,2] have made sparse semiconductor spin qubit arrays an appealing solid-state platform to realize quantum processors. The dynamic and long-range connectivity enabled by shuttling is also essential for many quantum error-correction (QEC) schemes. Here, we demonstrate a silicon spin-qubit device that comprises a shuttling bus for coherently transporting qubits that can interact at four isolated locations we call bus stops. We dynamically populate the array and tune all single- and two-qubit operations using shuttling and quantum nondemolition (QND) spin measurements, without access to charge sensing in most of the device. We achieve universal control of the effective five-qubit processor and select the connectivity required to form a surface-code stabilizer plaquette that supports X- and Z-type parity checks up to weightfour. We use the parity checks to generate multi-qubit entanglement between all qubit combinations in the array and report the genuine entanglement of a five-qubit Greenberger-Horne-Zeilinger (GHZ) state, constituting the largest such state ever constructed with gate-defined semiconductor spins. This work opens immediate opportunities to pursue QEC experiments [3] with spin qubits, and the protocols developed here lay the groundwork for the modular calibration and operation of sparse spin qubit arrays.

## References

[1] De Smet, M. et. al., Nat. Nanotechnol. 20, 866–872 (2025)
[2] Matsumoto, Y. et. al., arXiv:2503.15434 [quant-ph] (2025)
[3] Andersen, C.K. et. al., Nat. Phys., 16, 875–880 (2020)

## Figures

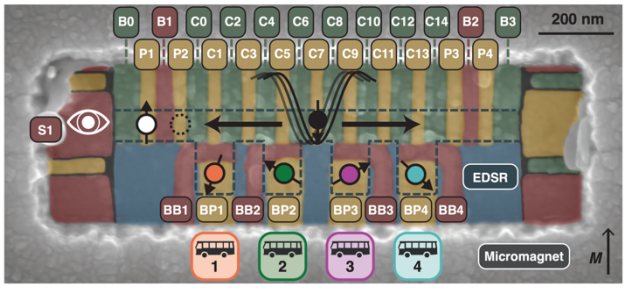


**Figure 1:** A sparse five-qubit bi-linear device connected with a conveyor shuttling channel for long range connectivity.

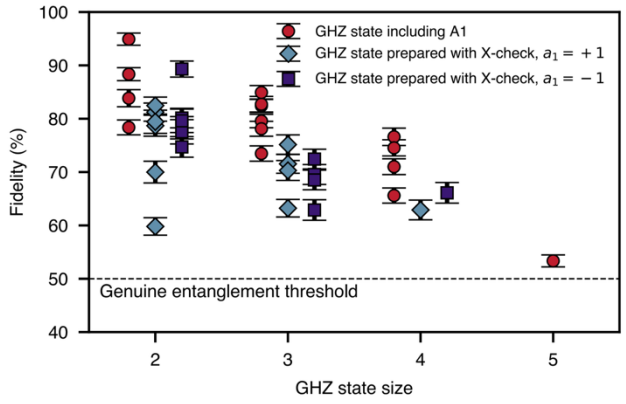


**Figure 2:** GHZ state fidelities for all combinations of two or more qubits in the five-qubit processor