

A High-Precision 698 fs RMS Phase Alignment of FPGA Transceivers for High-Repetition-Rate QKD Systems

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Abstract

Since the seminal BB84 protocol was proposed [1], quantum key distribution (QKD) has advanced rapidly, achieving landmark milestones including intercontinental satellite-ground key distribution [2]. For >1.25 GHz high-repetition-rate QKD systems, sub-10 ps phase synchronization is essential to sustain low quantum bit error rate (QBER), as >10 ps misalignment drastically degrades system extinction ratio [3].

Traditional GHz-level pulse generation relies on costly, bulky arbitrary waveform generators (AWGs), hindering QKD terminal miniaturization. FPGAs with embedded high-speed transceivers are promising cost-effective alternatives, yet their independent clock networks introduce stochastic phase skews at initialization—catastrophic for synchronous QKD. Existing solutions fail to meet stringent requirements: the PI-TDC architecture in [4] shows 12 ps RMS jitter and ~20 ps adjustment steps, failing sub-10 ps specifications.

In this work, we propose a metastability-referenced phase alignment architecture, locking clock phases to the narrow TDC metastability transition region instead of steady-state bins. Implemented on a 28-nm Virtex-7 FPGA, our design achieves 698 fs RMS jitter, 3.4 ps peak-to-peak jitter, 1.58 ps adjustment steps with <1% resource

consumption, and maintains QBER <0.45% in a 1.25 GHz QKD system across repeated power cycles.

References

- [1] Bennett, C. H., Brassard, G., Proceedings of IEEE International Conference on Computers, Systems, and Signal Processing, (1984) p. 175
- [2] Li, Y., et al., Nature, (2025) pp. 1-8
- [3] Li, Y., et al., Opt. Lett., vol. 44, (2019) p. 5262
- [4] Xie, H., Li, Y., Shen, Q., Liao, S., Peng, C., IEEE Trans. Nucl. Sci., vol. 66, (2019) p. 1070

Figures

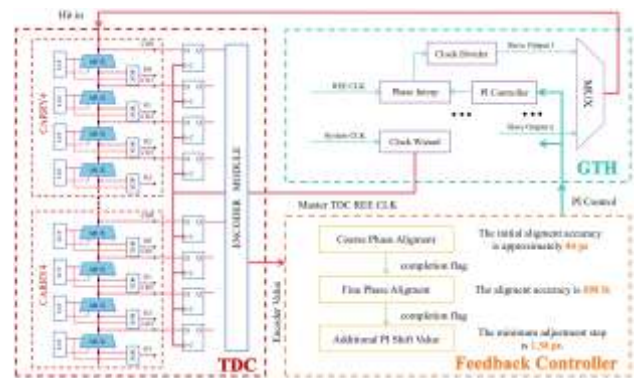


Figure 1: Block Diagram of the Temporal Synchronization Scheme.

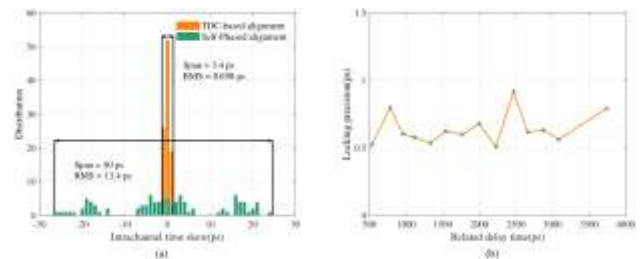


Figure 2: (a) Comparison of Temporal Synchronization Accuracy Between Different Schemes (b) Temporal Synchronization Accuracy of the Proposed Scheme Under Different Time Offsets