Advances in Material Characterization for Improving Semiconductor Spin Qubit Devices

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Semiconductor spin qubit devices for quantum computing applications have recently made rapid progress due to improvements in fabrication process control [1-5]. Nevertheless, such devices still suffer from heating, resonant drive and addressability challenges, as well as charge noise, jumps and drifts in the electrostatic environment that inhibit scaling to a useful number of functional qubits. Our research is focussed on improving materials analysis and circuit designs for such cryogenic applications [6]. Figure 1 shows a schematic of a spin qubit device highlighting a variety of areas of potential material improvement, such as (1) micromagnets, (2) metal gate resistivities and (3-4) gate oxides.

In this work, we will discuss recent results in those different areas. (1) The cryogenic measurement and simulation of on-chip micromagnets used to provide qubit addressability and driving gradients. (2) The pitch dependent resistivity values of metallic interconnects. (3) The temperature-dependence of permittivity and leakage properties of dielectrics. (4) The measurement of the density and energy levels associated with trap states present in an amorphous aluminum oxide gate dielectric. Figure 2 shows some preliminary data of palladium (Pd)-based resistivity of the interconnects.

Our aim is to create materials report cards that can be generated for each fabrication round. As such, it can be used to assess process control in fabrication as well as provide correlations between materials properties and spin qubit performance metrics.

References

[1] P. Steinacker et al., Nature 646 (2025) 81
[2] M. De Smet et al., Nat. Nanotech, 20 (2025) 866
[3] H. C. George et al., Nano Lett. 25 (2025) 793.
[4] Sieu D. Ha et al., PRX QUANTUM 6 (2025) 030327
[5] A. M. J. Zwerver et al.,, Nat. electronics, 5 (2022) 184
[6] R. Verberk et al., Proc. of SPIE Vol. 12472, 1247207.

Figures

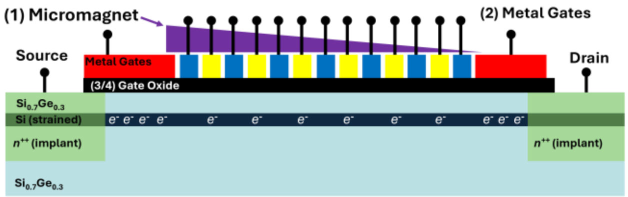

Figure 1: Schematic of a silicon spin qubit device highlighting some of the materials challenges reported as (1) micromagnets, (2) metal gate resistivities, (3-4) gate oxides. These activities are taking place at TNO together with our collaborators.

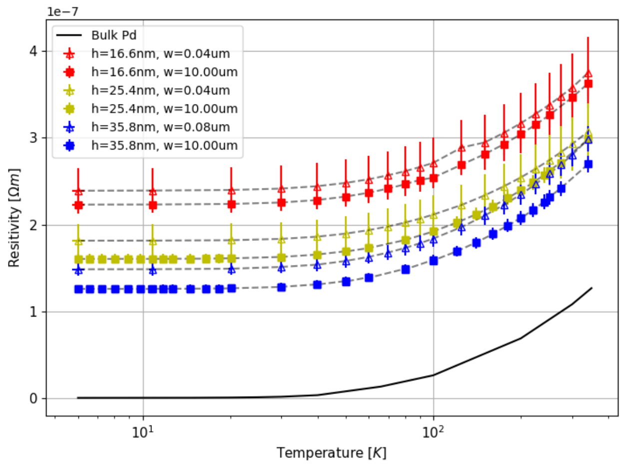

Figure 2: The resistivity of Pd interconnects used in the fabrication of spin qubit devices. Two widths (w) and different heights (h) of the interconnects were used. The symbols and colors correspond to the heights and widths of the interconnects, respectively.