Matchgate synthesis via Clifford matchgates and T gates

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As quantum processors approach early fault-tolerance, compiling a target unitary into a **discrete logical gate set** becomes a central challenge [1]. In many leading error-correcting codes, Clifford operations are comparatively cheap, while non-Clifford resources —such as T gates— dominate the overhead, making T-count and T-depth key optimization targets [2]. This has driven major progress in Clifford+T synthesis. Separately, research into compilation within structured subgroups of the unitary group has progressed, such as for the Clifford group [3], where compact representations enable substantially improved scaling. In this work we focus on the **matchgate group** [4], a well-studied subgroup of the unitary group connected to free-fermionic (Gaussian) dynamics. Matchgate circuits admit an efficient description via polynomial-size orthogonal transformations on Majorana modes, and they remain classically simulable under standard input and measurement restrictions. Crucially, unlike Clifford circuits, matchgates can still generate non-stabilizer resources, making them attractive for **scalable benchmarking** that probes "magic" in fault-tolerant regimes. We develop a **matchgate-only synthesis framework**, addressing both approximate and exact compilation. First, we identify a discrete gate set that is universal within the matchgate group. We then leverage the compressed matchgate representation in $SO(2n)$ to perform compilation in an exponentially smaller space, and we provide rigorous guarantees relating approximation accuracy in the orthogonal representation to the induced error on the full quantum circuit. On the exact side, we characterize a broad family of exactly synthesizable matchgates and present an algorithm with runtime polynomial in system size. Finally, we show how optimal exact synthesis can be mapped to SAT and demonstrate the approach on matchgate circuits that diagonalize a free-fermionic Hamiltonian. Our results provide practical tools for compiling matchgate circuits at scale, with applications to fermionic simulation and to benchmarking protocols that remain efficiently verifiable while accessing non-stabilizer regimes.

References

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[3] S. Bravyi, R. Shaydulin, S. Hu, and D. Maslov, Quantum 5(2021) 580

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Figures

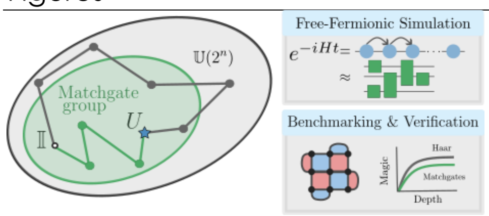

Figure 1: We synthesize matchgate unitaries using only matchgates, enabling compilation in a $2n \times 2n$ space rather than the full $2^n \times 2^n$unitary space. Our results may find applicability in free fermionic dynamics and in benchmarking and verification protocols.