Quantum Brilliance's Integrated Architectures for Deployable Diamond Quantum Technologies

Lykourgos Bougas
Simon Baber, David Collomb, Felix Engel, Jonas Foglszinger, Santiago Corujeira Gallo, Danial Majidi, Xaver Mooslechner, Mohammad Sajedi, Ayman Sakr, Jan Sonsky, Rishabh Yadav

Quantum Brilliance GmbH, Industriestraße 4, Stuttgart, Germany
lykourgos.b@quantum-brilliance.com

Abstract

Diamond Nitrogen-Vacancy (NV)-based quantum technologies offer room-temperature operation, long spin coherence times, and multi-quantity sensitivity [1], positioning them as strong candidates for practical quantum computing and sensing systems. Translating these advantages into edge-deployable products demands high-performance quantum devices and integration architectures meeting size, weight, and power (SWaP) constraints from chip to system level.

Here, we present two advances toward this goal. First, we introduce the Smart Diamond Chip (SDChip), a monolithically integrated diamond quantum device supporting application-specific NV configurations (NV ensembles for quantum sensing or dipolar-coupled arrays for multi-qubit computing) [2] co-integrated with all control structures required for quantum operations, such as static and gradient magnetic fields for spin conditioning and nanoscale-selective addressing, microwave and RF structures for electron and nuclear spin control, and metallic contacts for biasing and photocurrent-based state readout. And second, the Diamond Quantum System-in-Package (QSiP) that combines SDChip as the quantum processing core with co-packaged front-end chips covering microwave synthesis, generation and amplification, laser delivery, and optical detection. This multi-chip module approach eliminates bulky discrete components, enables ASIC-grade integration with SDChips, and achieves system-level SWaP performance that discrete implementations cannot match.

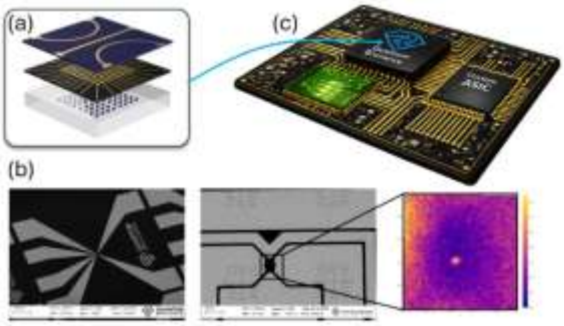

Figure 1: (a) Graphic of SDChip for quantum computing, depicting on-diamond MW/RF delivery lines and contact electrodes for the control and readout of NV-based multi-qubit 2D arrays. (b) SEM images of QB's on-diamond micro-coils and contact electrodes, alongside confocal image of NV centers precisely aligned within the structures. (c) Graphic representation of QSiP powered by a QB's SDChip.

We report progress across three fronts in relation to the SDChip and QSiP developments in Quantum Brilliance. First, advances in on-diamond metallization process modules, integrating multiple control structures with distinct critical dimension and interface requirements across multi-step lithography sequences, and their translation into functional SDChips. Second, characterization results from SDChip demonstrators evaluating high-performance quantum operations on single NV centers and multi-NV clusters, with results pointing toward performance regimes relevant to both sensing and computing. And third, preliminary QSiP architectures for quantum computing, covering system partitioning, key integration challenges, and building blocks under development toward a first prototype module.

References

[1] Doherty et al., Physics Reports **528.1** (2013) 1-45
[2] Oberg *et al., Mater. Quantum. Technol.* **5** (2025) 03300