Optimising the quality of gate dielectrics in Ge hole-spin qubit devices

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Continued advances in the fabrication of Ge/SiGe heterostructures have led to gate-defined hole spins in strained germanium layers being identified as a viable qubit platform [1, 2]. Advantages include a large spin-orbit interaction to allow all-electric control of the spin, a small effective mass to allow a more relaxed gate layout geometry, and a *p*-like orbital symmetry giving a reduced hyperfine interaction and thus favouring spin coherence. However, as the number of qubits is scaled up, increased focus on the uniformity of the device is required, whereby electrically-active defect states in the bulk and at interfaces can affect transport and introduce significant sources of decoherence [3, 4]. Careful control and optimisation of the device production process, including feedback loops at various fabrication stages, is thus an important task for qubit scale-up.

Here, we present outcomes from a series of experiments that focus on the role of the oxide as a medium for the trapping and emission of mobile charge carriers and thus contributing a significant source of charge noise. In the initial phase of investigation, test structures comprised of metal-oxide-semiconductor (MOS) capacitors on Si are used to evaluate the magnitude of fixed oxide charge Q_f and interface trap density D_{it}. We show that through careful optimisation of the atomic layer deposition parameters, as well as incorporating various pre- and post-oxidation treatments, D_{it} and Q_f can be reduced below 2×10^{11} eV^{-1} cm^{-2} and 1×10^{12} cm^{-2}, respectively. Next, we move to a $Ge_{0.7}/SiGe_{0.3}$ substrate, the heterostructure stack used for quantum dot devices. In addition to MOS capacitors, we fabricate test structures comprising multiple depletion gates in order to probe charge disorder on the nanoscale. Here we show the benefits that post-oxidation and post-metallisation annealing bring in terms of reduced hysteresis and increased uniformity of the pinch-off voltages. All together, these results point to an optimised fabrication process flow that reflects a minimum in the amount of electrically-active defect states and thus a favourable environment for which to host large-scale qubit arrays in a relatively noise-free setting.

References

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[3] M. J. Carballido et al., arXiv:2404.07313 (2024)
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Figures

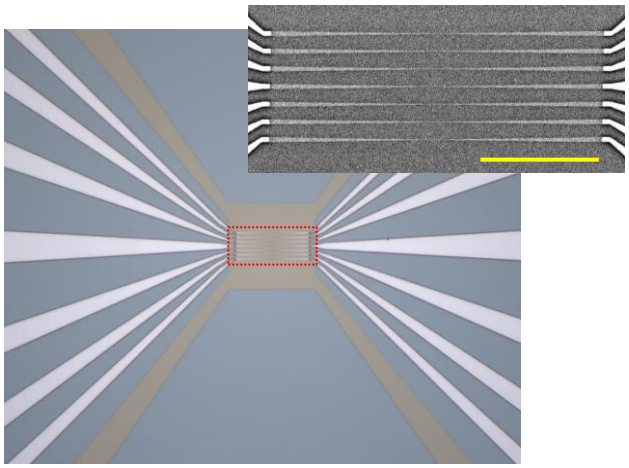

Figure 1: Optical/SEM images of a test structure comprising 7x Ti/Pd depletion gates fabricated on a Ge/SiGe substrate. Scale bar = 5 µm