Quantum Device Integration in Ge/SiGe heterostructure

Matteo Orlandoni
Benoit Bertrand
Silvano Defranceschi
Jean-Michel Hartmann
Vivien Schmitt
Frederic Gustavo
CEA-Leti, 17 Av. des Martyrs, *Grenoble, France*
matteo.orlandoni@cea.fr

Semiconductors Quantum Dots (QDs) [1] have emerged as a promising candidate for quantum information processing, opening up the possibility of encoding information in the spin states of charges. This has led to research for new and performing materials to host QDs. In that context, Ge has emerged as a promising candidate in quantum technologies, particularly gaining attention as a platform for spin qubits, gatemons, and topological states applications.
Among the different Ge platform that can be studied and exploited [2], we focus on Ge/SiGe heterostructures, consisting in a thin strained layer of Ge (<20 nm) grown between two layers of $Si_{0.2}Ge_{0.8}$.
Different Ge/SiGe wafers were fabricated in CEA-Leti cleanrooms, differing in the thicknesses of the Ge quantum well, SiGe spacers and the surface cap.
To benchmark these wafers, we performed 4K Hall bar (HB) measurements for systematic extraction of mobility and percolation density.
These test-structures were fabricated in PTA-cleanrooms following two specific recipes for surface preparation before the gate stack deposition. All HB measurements were conducted under low magnetic fields, low temperatures, and with a DC bias applied. Every HBs highlighted a peak mobility always higher than 1.10^5 $cm^2/V.s$, suggesting a high epitaxial growth quality. The percolation density was found to be below 5.10^{10} cm^{-2} for all devices, again proving the low disorder properties of the heterostructures. The results also highlighted that the use of an O_2 plasma treatment during the surface preparation results in a lower mobility and higher percolation density, indicating that it actually tends to deteriorate the surface. This result highlights how the surface quality is a key parameter for optimizing the device performance.

References

[1] Loss, Daniel and DiVincenzo, David P., Phys. Rev. A 57,1 (1998) ,120 –126
[2] Scappucci, Giordano *et al.*, *Nature Reviews Materials*, **6**, 926-943 (2021)

Figures

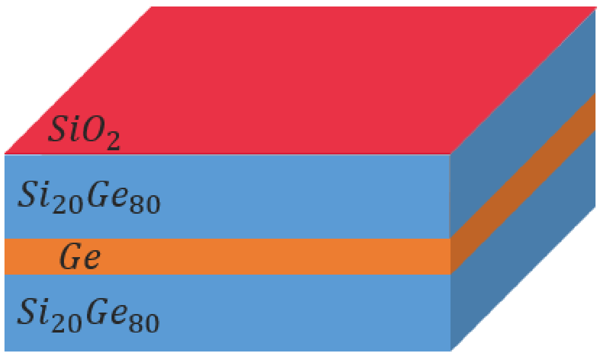

Figure 1: Schematic of a Ge/SiGe heterostructure.

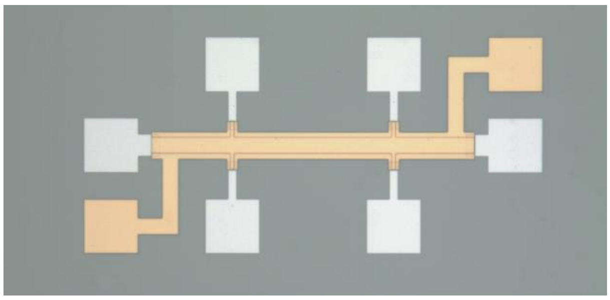

Figure 2: Picture of a single Hall Bar fabricated at PTA facility.