High-fidelity gates and readout for superconducting quantum processors

Yasunobu Nakamura

RIKEN Center for Quantum Computing, Wako, Saitama, Japan
Department of Applied Physics, Graduate School of Engineering, The University of Tokyo, Bunkyo-ku, Tokyo, Japan

yasunobu@ap.t.u-tokyo.ac.jp

Quantum computing demands an unprecedentedly high level of precision in the control and readout of quantum states encoding quantum information in a large Hilbert space. Therefore, in parallel with the pursuit of scalability, persistent efforts have been made to improve control and readout fidelities of qubits. We are developing two-dimensionally integrated superconducting qubit arrays for quantum computing. In our architecture, unit cells consisting of four qubits and a four-fold-multiplexed readout port are tiled to produce a larger array. The control and readout signals are delivered vertically from the backside of the chip. This talk will also cover our approaches toward fast multiplexed qubit readout [1] and fast two-qubit gates using a tunable coupler between fixed-frequency qubits [2]. The fidelities above 99.9% have been reached, and further improvements are awaited.

References

[1] P. A. Spring *et al.*, arXiv:2409.04967.
[2] R. Li *et al.*, Phys. Rev. X 14, 041050 (2024).

Figures

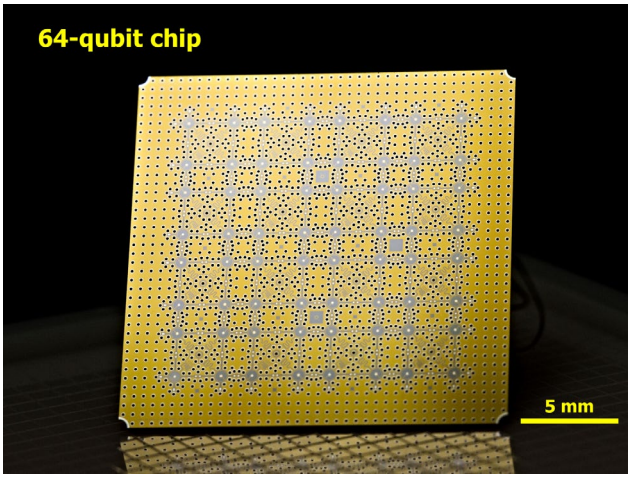

Figure 1: Picture of a 64-qubit superconducting quantum processor chip

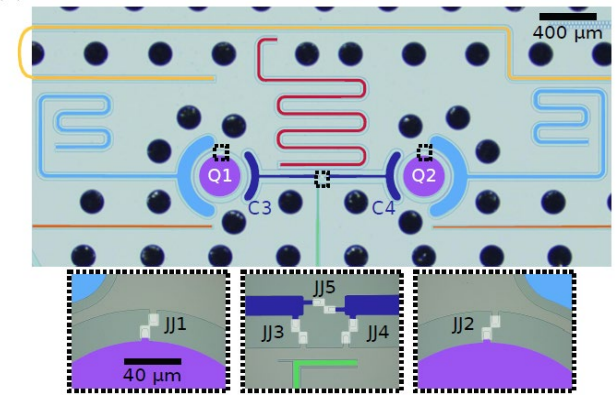

Figure 2: False-color image of a two-qubit chip for the demonstration of a high-fidelity CZ gate with a douple-transmon coupler [2].