Steps towards variability-resilient spin qubits

Biel Martinez[1]
Silvano DeFranceschi[2], Yann-Michel Niquet[3]

1. Univ. Grenoble Alpes, CEA, LETI, F-38000, Grenoble, France
2. Univ. Grenoble Alpes, CEA, Grenoble INP, IRIG-PHELIQS, F-38000, Grenoble, France
3. Univ. Grenoble Alpes, CEA, IRIG-MEM-L_Sim, F-38000, Grenoble, France

biel.martinezidiaz@cea.f

The scalability of semiconductor spin qubits will undoubtedly face the challenge of ensuring clean enough environments to host qubits with homogeneous properties all across the quantum processors. In this sense, epitaxial heterostructures appear advantageous with respect to MOS-based counterparts [1] due to the crystalline nature of their interfaces. Holes in Ge/SiGe heterostructures experience a wide variety of SOC mechanisms [2-4], which can be leveraged for electrical spin manipulation, but also enhance the sensitivity to electrical disorder [5].

In this work, we performed numerical simulations to quantify the variability on the charge and spin properties of Ge spin qubits, evaluate its impact on the scalability perspectives of this platform, and explore actions to mitigate it. While variations in the charge properties remain moderate, spin properties still suffer from significant variability (see Figure 1). Nonetheless, the bounds for interface quality are highly constraining for large-scale architectures (see Figure 2). We showe that these constraints could be released via strain engineering [6] and gate layout optimisation [7], reaching manageable variability levels at achievable interface qualities.

References

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Figures

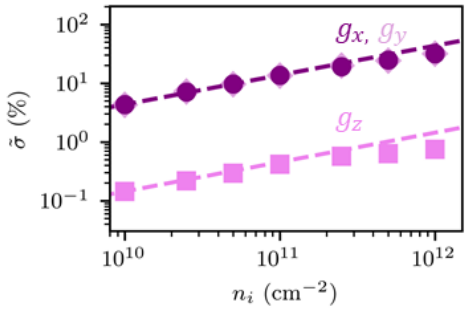

Figure 1: Relative standard deviation of the in-plane (g_x, g_y) and out-of-plane (g_z) effective g factors as a function of the charge trap density (n_i) at the top SiGe interface of a prototypical Ge spin qubit device.

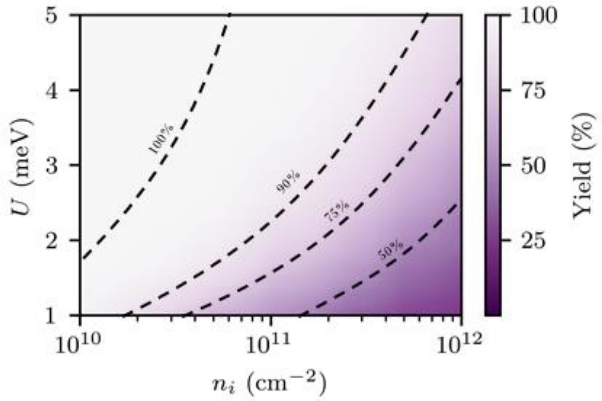

Figure 2: Predicted percentage of devices with single-hole occupancy as a function of the charge trap density (n_i) and the qubits charging (U) energy in a device with shared plunger gate voltages.