Automatic Compilation of Dynamic Circuits

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We present a novel framework for generating dynamic quantum circuits that automatically prepare any state or unitary operator. This procedure is powered by numerical optimization-based circuit synthesis methods. The first contribution is introducing optimization objective functions to exploit mid-circuit measurement and feed-forward operations. The second contribution is incorporating these into a popular open-source quantum circuit synthesis framework. We demonstrate the generation of state preparationcircuits, long-range entangling gates, circuit optimization, and the application of dynamic circuits to lattice simulations. The resulting circuits are validated through simulation as well as through execution on quantum hardware. Furthermore, we perform noise analysis to explore the impact of different error ratios in mid-circuit measurements and gate errors, identifying scenarios where dynamic circuits offer the most significant benefits. The dynamic circuits generated by our framework show substantial improvements in reducing circuit depth and, in some cases, the number of gates required. To our knowledge, this is the first practical procedure to generate dynamic quantum circuits. Our objective functions are independent of the underlying synthesis framework and can be easily reused. The framework opens new possibilities for circuit generation and optimization methods, and the current results highlight the potential of dynamic circuits to enhance the performance of quantum algorithms on quantumcomputers.

References

[1] Siyuan Niu et al. AC/DC: Automated Compilation for Dynamic Circuits. https://arxiv.org/pdf/2412.07969

Figures

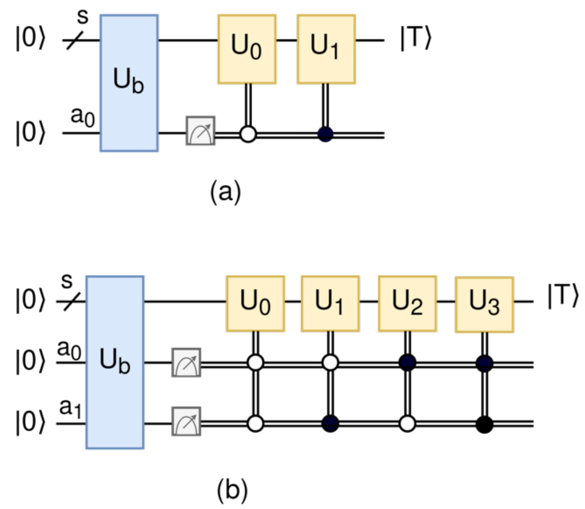

Figure 1: Dynamic circuit protocol for preparing a target state **|T⟩** using (a) 1 ancilla and (2) 2 ancillas with simultaneous measurement in one cycle. ***S*** denotes the system qubits and $\boldsymbol{a_i}$ denotes the ancilla qubits. It is easy to extend the protocol to arbitrary number of ancillas. The goal is to determine $\boldsymbol{U_b}$ and $\boldsymbol{U_i}$ for $\boldsymbol{i= 0,\dots,2^{a-1}}$

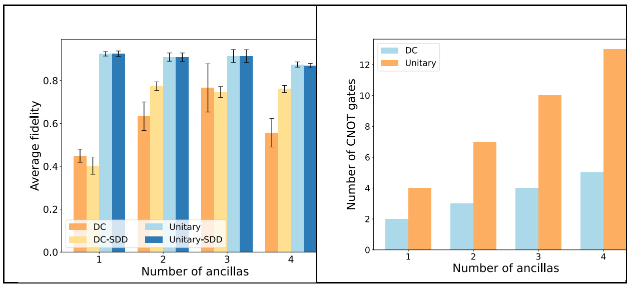

Figure 2: Fidelity results for executing unitary and dynamic circuits to prepare long-range CNOT gate on linear chain on IBM quantum hardware, together with the number of CNOTs in the circuit. The total number of qubits is the number of ancillas plus 2 data qubits, with the long-range CNOT applied to the first and last qubits (data qubits) and the ancilla qubits in between. SDD represents staggered dynamical decoupling.