Alternative Superconductors to Aluminum for Gate-Tunable Hybrid Josephson Junctions

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Today, substantial efforts are made to develop epitaxial superconductor thin films on semiconductors. These hybrid heterostructures hold promise for enabling error-limited quantum computation through qubits with longer coherence times, as well as topologically protected qubits. This began with the quest for improved material interfaces for gate tunable proximity effect, and in particular with the development of in-situ epitaxial aluminum (Al) shells on InAs nanowires. However, Al is limited in terms of critical current and superconducting gap. Additionally, many other superconductors remain underexplored.
Here, we present our efforts to develop expertise in alternative superconductors such as tin (Sn) and tantalum (Ta). Both materials are known for having higher superconducting gap than Al. However, both are allotropes, meaning they can exist in multiple crystalline phases, with only one phase being suitable for qubit technologies. Therefore, significant work is needed to control the crystalline phase of Sn and Ta during epitaxy or deposition to favor the desired phase. Additionally, it is critical to ensure that interfaces remain undamaged during the growth process.

For instance, Sn has a superconducting β-phase, which is tetragonal, while its α-phase is cubic and behaves as a semimetal. Using X-ray diffraction (XRD) and transmission electron microscopy (TEM), we demonstrated that forming the β-phase of Sn on III-V semiconductors is non-trivial, particularly when depositing thin films at cryogenic temperatures [1,2]. Devices fabricated from Sn/III-V nanowires are gate tunable, exhibit high critical currents and strong resilience to magnetic fields [1,3]. Finally, these hybrids are ideal building blocks for integration into Josephson parametric amplifiers, gatemons, and Majorana-based systems.
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References

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Figures

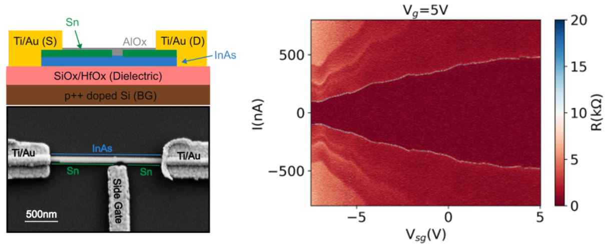

Figure 1: Left: vertical cross-section through a device (not to scale) and SEM image of a nanowire device. Right: dV/dI as a function of current bias and side gate voltage, with the backgate voltage fixed at V_{bg} = 5V.