FDSOI Spin Qubit Device optimization

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Silicon spin qubits based on Fully Depleted Silicon-On-Insulator (FDSOI) present a promising approach for scalable quantum computing, leveraging their compatibility with existing semiconductor manufacturing production lines for efficient industrial adoption. These qubits are typically formed in electrostatically defined quantum dot arrays, requiring precise control over chemical potentials and tunnel couplings for effective operation. We report on advancements in fabrication techniques and novel device architectures that enhance qubit readout sensitivity while minimizing parasitic couplings in silicon nanowire structures.

To achieve fine electrostatic control over the quantum dot array, we implement pitch doubling with a second gate layer [1], enabling precise tunability of the tunnel couplings and charge configurations. Additionally, we introduce two self-aligned gate-active patterning schemes [2]: the dashed nanowire (NW) configuration, which selectively removes silicon in diagonal inter-gate regions to suppress unwanted tunnel couplings while maintaining charge sensing compatibility, and the dual nanowire (NW) configuration, which separates the two sides of the qubit array to eliminate transverse coupling, improving qubit isolation. These fabrication enhancements, developed using commercially viable semiconductor processes, allow for greater quantum dot control while ensuring manufacturability.

Low-temperature measurements confirm that tunnel coupling modulation can be achieved across multiple orders of magnitude in both the many- and few-electron regimes. Numerical simulations also suggest that charge detection sensitivity can be significantly improved following realistic design optimization, supporting high-fidelity qubit readout essential for scalable quantum computing applications.

References

[1] T. Bédécarrats et al., IEDM, (2021)
[2] B. Bertrand et al., IEDM, (2023)

Figures

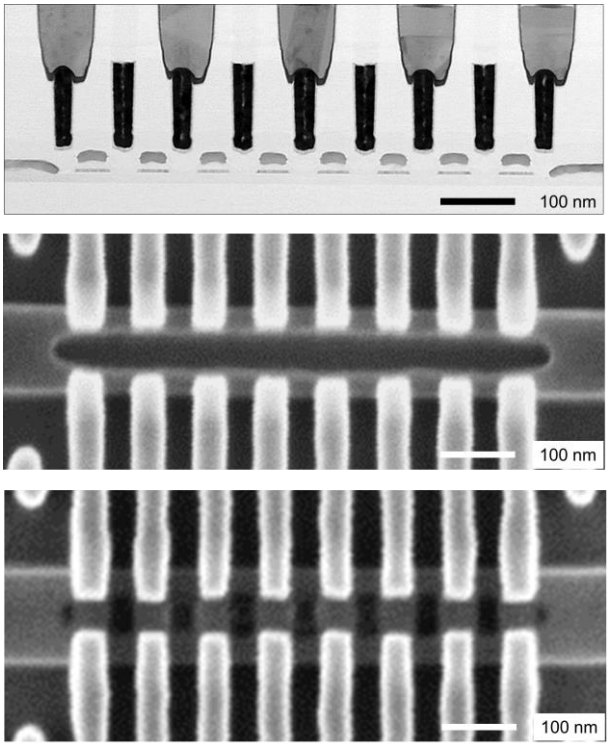

Figure 1: TEM and SEM images of the fabricated devices illustrating the pitch doubling strategy and the different self-aligned gate-active patterning schemes.