Interconnect Properties of Spin Qubit Devices

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Significant progress in the control of single electrons in semiconductor quantum computing devices has been recently shown [1, 2]. However in order to scale such systems to larger qubit counts the improved control of materials properties will be critical. In this work we show room temperature characterization of multi-layered test structures fabricated on the same chip as spin qubit devices [3]. We observe that on-chip palladium interconnects have higher sheet resistances than palladium as deposited. Such additional resistance could be responsible for qubit "heating" during cryogenic device operation [5]. We also show the voltage- and frequency-dependent dielectric properties for the amorphous alumina (Al_2O_3) material used as the interlayer dielectric and gate oxide in our spin qubit devices (Fig. 2). Such dispersive behaviour may contribute to charge noise and/or device drift. Finally, we also discuss our recent developments in the magnetic material of the nanomagnets used for qubit addressability.

References

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[2] Xue et al., Nature, 601 (2022) 343.
[3] Verberk et al., Proc. SPIE 12472, 37th European Mask and Lithography Conference, 1247207 (2022) 1.
[4] de Vries et al., Thin Solid Films, 167 (1988) 25.
[5] Undseth et al., Physical Review X,13 (2023) 041015.

Figures

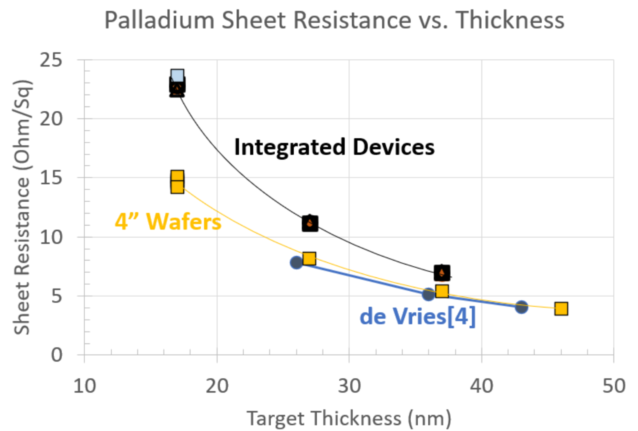

Figure 1: The sheet resistance values of test structures integrated during fabrication of qubit device runs (black and blue squares) are larger than the values of as-deposited palladium test wafers (yellow squares), which are similar to those reported in de Vries [4].

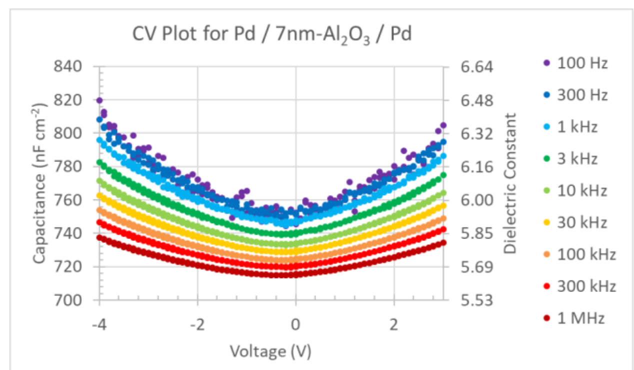

Figure 2: Frequency and voltage dependence of capacitance data for a 7 nm amorphous Al_2O_3 film between palladium electrodes.