Look-up table based fast tune-up of superconducting quantum processors.

Thijs Stavenga
Thijs Stavenga, Roald van den Boogaard, Floris Brullemans, Arno Bargerbos and Marten Arthers

Quantware, Electronicaweg 10, Delft, The netherlands

thijs@quantware.com

In recent years, the size and complexity of state-of-the-art quantum devices has increased significantly. The large number of qubits and peripherals demand the optimization and implementation of an ever growing number of parameters into circuit geometry. Additionally every qubit has several parameters that have to be implemented into a geometry to obtain the correct capacitance. However, simulating and optimizing the geometry using finite element methods is time prohibitive and does not scale to larger devices. Here, we present an alternative way of optimizing the circuit geometry using a pre-simulated look-up table to yield the desired circuit. Using the look-up table we get an optimization speedup of 3 orders of magnitude, bringing back the time from days to minutes, without significantly affecting parameter accuracy. This proves the look-up table to be a scalable way to implement the desired Hamiltonian parameters into circuit geometries.