Addressing the scalability of quantum annealing of classical problems

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Quantum annealers are often presented as application-specific devices intended to harness quantum effects to solve classical optimisation tasks. This is due to the connection between the Ising model and QUBO (Quadratic Unconstrained Binary Optimisation) problems, to which several problems of interest can be mapped. However, the hard-wiring of a fully connected graph, a general requirement for these problems, is not scalable due to crosstalk and packing issues within the chip. We present a scalable architecture to embed an all-to-all connected Ising model within another Ising model defined on a graph of degree d = 3 containing exclusively 2-local interactions. This essentially amounts to an efficient braiding of logical chains of qubits which can be derived from a description of the problem in terms of triangles, naturally linking to a family of equivalent formulations of an Ising instance. We also devise strategies to address the challenges of scalable architectures, such as the faster shrinking of the gap due to the larger physical Hilbert space and the scaling of penalty strengths [1, 2], in the specific context of our architecture. These strategies consist on driver Hamiltonians that are more suited to the symmetries of the logical solution space, extending ideas from [3, 4]. The hereby proposed architecture opens an alternative route to scale up devices dedicated to classical optimization tasks within the quantum annealing paradigm.

References

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Figures

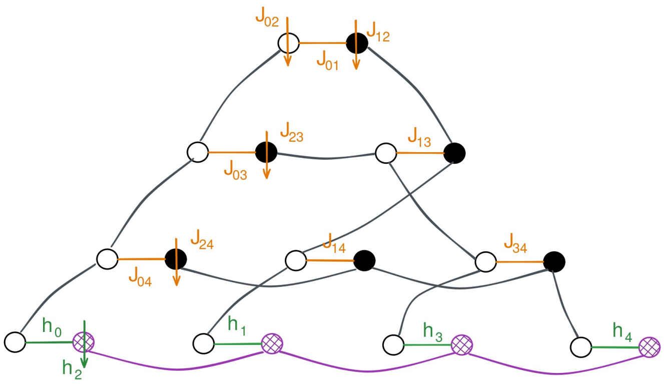

Figure 1: Schematic of the architecture for N=5 incorporating local fields.

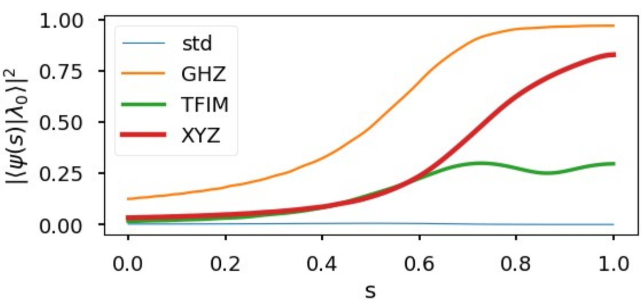

Figure 2: Success probability of finding the logical ground state along the anneal in a small example (3 logical variables, 9 physical qubits) for different driver Hamiltonians for an instance in which the logical ground state is in the (degenerate) 4th-excited manifold of the embedding Hamiltonian.