Comparative study of quantum error correction strategies for the heavy-hexagonal lattice

César Benito, Esperanza López, Borja Peropadre, Alejandro Bermudez

Topological quantum error correction is a milestone in the scaling roadmap of quantum computers, which targets circuits with trillions of gates that would allow running quantum algorithms for real- world problems. The square-lattice surface code has become the workhorse to address this challenge, as it poses milder requirements on current devices both in terms of required error rates and small local connectivities. In some platforms, however, the connectivities are kept even lower in order to minimise gate errors at the hardware level, which limits the error correcting codes that can be directly implemented on them. In this work, we make a comparative study of possible strategies to overcome this limitation for the heavy-hexagonal lattice, the architecture of current IBM superconducting quantum computers. We explore two complementary strategies: the search for an efficient embedding of the surface code into the heavy-hexagonal lattice, as well as the use of codes whose connectivity requirements are naturally tailored to this architecture, such as subsystem-type and Floquet codes. Using noise models of increased complexity, we assess the performance of these strategies for IBM devices in terms of their error thresholds and qubit footprints. An optimized SWAP-based embedding of the surface code is found to be the most promising strategy towards a near-term demonstration of quantum error correction advantage.

arXiv:2402.02185