Scaling spin qubit devices: vertical interconnects through Al_2O_3

H.G.J. Eenink[1]
S.V. Amitonov[1], S.D. Oosterhout[1], L Tryputen[1], A. Sammak[1], D.J. Michalak[1], F. Borsoi[2], V.John[2], L.E.A. Stehouwer[2], M.W.H. De Smet[2], Y. Matsumoto[2], G. Scappucci[2], L.M.K. Vandersypen[2], M. Veldhorst[2]

1 QuTech and TNO Netherlands Organisation for Applied Scientific Research, Stieltjesweg 1 2628 CK, Delft, Netherlands
2 QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1 2628 CJ, Delft, Netherlands
gertjan.eenink@tno.nl

To successfully scale quantum devices to larger numbers of qubits, the fabrication toolkit needs to be expanded. While conventional semiconductor devices use multi-layered metal lines with vertical interconnects, this technique is not yet adapted and employed for quantum devices. We have developed two processes for this purpose, first an etching and metallization process that enables vertical connection through Al_2O_3. This functionality enables an upgrade of current devices [1] to perform conveyor-mode single electron shuttling in Si/SiGe [2] over distances of 10 µm and more. 8 sets of 15 gates each can be contacted in parallel. In addition, we have adapted platinum germanosilicide ohmic contacts [3] for small footprints of ~200x200 nm. In combination with vertical contacts, this enables advancing dense 2D arrays of Ge/SiGe quantum dots [4] by integration of a single electron transistor charge sensor inside the array. In this talk we will describe the development, challenges and results of both processes, and show how characterization of the diffusion process allows us to ensure low-resistance contact to the quantum well. Finally we will discuss the implications for the scaling of quantum devices.

References

[1] Zwerver, A.M.J. et al., PRX Quantum 4, 030303 (2023)
[2] Seidler, I. et al., npj Quantum Inf 8, 100 (2022)
[3] Sammak, A. et al., Adv. Funct. Mater. 29, 1807613 (2019)
[4] Borsoi, F. et al., Nat. Nanotechnol. 19, 21-27 (2024)

Figures

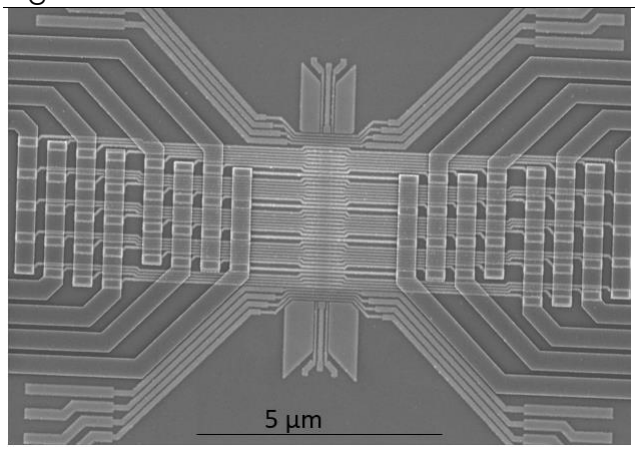

Figure 1: SEM image of conveyor gates spanning 3 µm. 8 sets of Ti/Pd gates are contacted by vias.

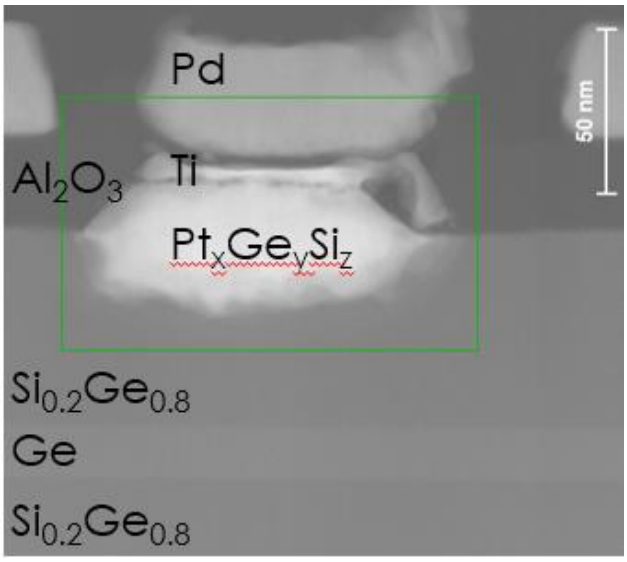

Figure 2: TEM image of nanoscale platinum germanosilicide ohmic contact. Platinum diffuses partly into the SiGe buffer.