Spin Qubits produced with a 300mm fabrication line: An update on Intel Si/SiGe devices

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Abstract
Quantum computing holds the possibility of de-livering exponentially more computing power for some applications than today's largest supercom-puters. While many different qubit technologies exist, only spin qubits map to a fab transistor process. In this presentation, we present an update on the progress of Si/SiGe Qubits fabricated using the standard tools of Intel's latest technology node.

Introduction

The qubit is the fundamental device of a quantum computer. It is the equivalent to the transistor in CMOS logic devices. And while it took the semicon-ductor industry 42 years from the first transistor to the first 1M transistor microprocessor, the quantum commu-nity hopes to reach this milestone much faster. But there are no less than 10 qubit types and most require new materials and new inventions to realize even a few qubits. Of these qubit types, only spin qubits in silicon are similar to transistors and are compatible with the infrastructure of advanced CMOS fabrication. By leveraging all of the work in transistor fabrication, we can perhaps shorten accelerate the time. - The future of quantum computing starts with a grain of sand.

Spin Qubits

Spin qubits are similar in geometry to a conventional, planar transistor but are operated in the single electron regime and under a magnetic field. The two level system or 0 and 1 of the spin qubit is determined by the spin state (up/down) of a single electron and enables the one qubit gates of a quantum computer. Two qubit gates are achieved by controlled overlap of electron wavefunctions between adjacent qubits (transistors).

At Intel, we fabricate silicon-based quantum compu-ting devices in the same advanced 300mm fab where our next generation process technology is developed. In-tel's quantum hardware group has released a new silicon spin qubit test chip, Tunnel Falls, a 12-quantum-dot line-ar array fabricated using Intel's D1high-volume manu-facturing line. Tunnel Falls incorporates standard micro-electronics design, materials, and fabrication techniques including EUV li-thography for the patterning of tight pitch device features. (See Figures 1,2)
In this talk we will share a general overview of spin qubit devices and Intel's test chip.
We will then present qubit performance benchmarking of multiple qubit encodings on these Si/SiGe spin qubit devices. Finally, we will discuss how results from this work are being used to vali-date design features, device physics, and fabrication pro-cesses that are being tested in extensible arrays for future technologies.

Figures

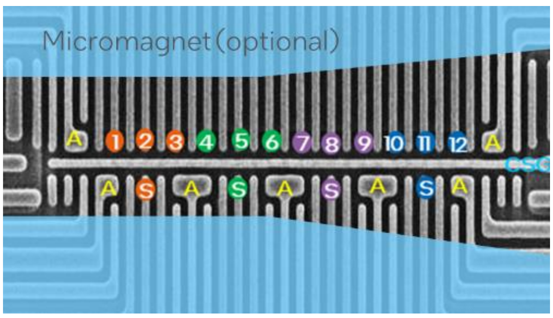

Figure 1: Top-Down SEM of a 12 "dot" linear array. Individual Gate wires (top) act as plungers and barriers to accumu-late single electrons under adjacent gates while "sensor dots" (bottom) can detect the spin of the electron in the qubit.

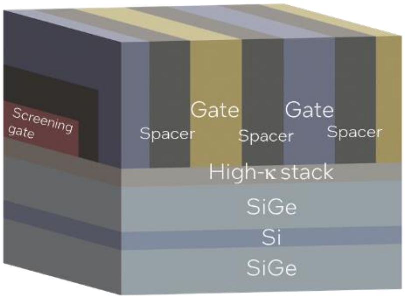

Figure 2: Cross section schematic of a spin qubit gate array fabri-cated through industry standard processes.