Tunable-coupler mediated multi-qubit controlled-phase gates with superconducting qubits

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Applications for noisy intermediate scale quantum computing devices rely on the efficient entanglement of many qubits to reach a potential quantum advantage. Entanglement is typically generated using two-qubit gates, with the qubits arranged on a square grid with pair-wise qubit-qubit couplers. Using fixed-frequency transmon-type qubits in combination with flux-tunable couplers allows to realize high coherence qubits with well controllable interactions. Tuning the frequency of the coupler by adiabatic flux pulses enables us to control the conditional energy shifts between the qubits and to realize controlled-phase [1,2]. In this system we optimize the pulse performance by analyzing and optimizing pulse shape parametrization in simulation and closed-loop experiments to realize decoherence limited CPHASE gates.
For the direct implementation of strong multi-qubit interactions, we further extend the scheme to a coupling of three qubits via a single coupler [3]. Here, the full family of pairwise controlled-phase (CPHASE) and controlled-controlled-phase (CCPHASE) gates can be implemented. We describe a gate protocol consisting of adjustable interactions and refocusing pulses. Numerical simulations result in CCPHASE gate fidelities around 99% for typical system parameters and decoherence rates.

References

[1] M. C. Collodo et al., Phys. Rev. Lett. 125, 240502 (2020).
[2] Y. Xu et al., Phys. Rev. Lett. 125, 240503 (2020).
[3] N. J. Glaser, F. Roy, and S. Filipp, Phys. Rev. Appl. 19, 044001 (2023)

Figures

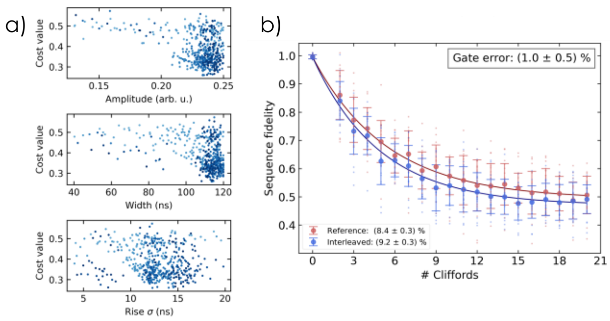

Figure 1: a) Closed-loop optimization of adiabatic two-qubit CPHASE gate, with the evolution of the gate parameters (pulse amplitude, shape width and rise time σ). b) Interleaved randomized benchmarking of optimized gate.

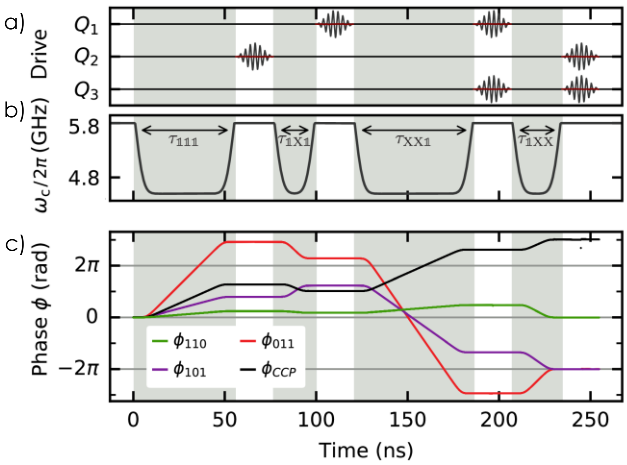

Figure 2: Pulse sequence of adiabatic three-qubit CCPHASE gate with a) microwave drives on the qubits and b) flux tuning of the tunable coupler. c) Evolution of the relative phases during gate execution.