Quantum Intranets for Scalable Multi-Core Quantum Computing

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The unprecedented power of Quantum Computing (QC) has been lately accelerating its endeavour from the theory to the experimental demonstration [1]. However, the complexity and resource-intensive nature of current quantum processors make every qubit count, and scaling up to the qubit numbers that are needed to unlock the full potential of QC is proving to be a considerable obstacle to surmount [2]. Together with research on improving qubit isolation and control, multi-core quantum processors have been proposed as a solution to these scalability issues [3]: interconnecting current quantum chips with dozens of qubits each (Fig. 1) with experimentally demonstrated chip-to-chip quantum state transfers (using e.g. ion shuttling or qubit teleportation)[4] in a quantum intranet is envisioned to be the"quantum leap" that will unleash QC performance. Nevertheless, coordinating several independent quantum processors comes with its own share of challenges. Communicating quantum data, which cannot be copied and is steadily corrupted, implies an environment where latencies play a leading role, thus affecting the overall computation performance. Because of this, we postulate that to lay firm foundations for multi-core quantum computing architectures, a deeply entangled design between quantum communication and computation is essential. Much work is being done on large-scale quantum communications and the Quantum Internet [5], yet a gap exists covering chip-scale quantum communications for QC. In our oral presentation, we propose a double full-stack layered vision combining communications with single-chip quantum computer designs (Fig. 1). This approach lets us perform thorough design explorations of these systems in order to derive the minimum requirements for the quantum-coherent inter-core interconnect that will ultimately unlock QC scalability.

Figures

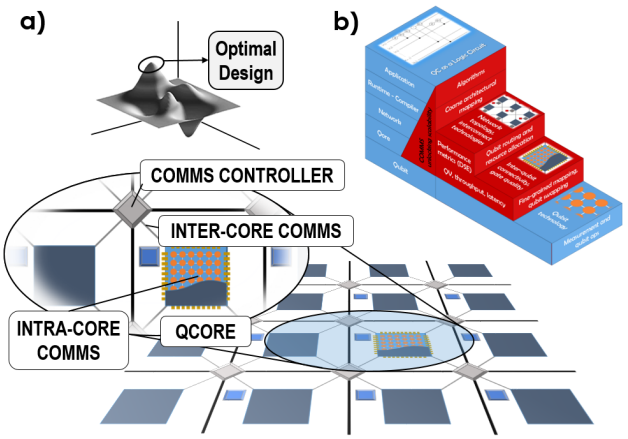

Figure 1: Multi-core quantum platform vision.
a) 3D diagram of a multi-CORE architecture
b) Double layered full-stack architecture

References

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