Benchmarking quantum error correcting codes on near-term devices

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Abstract

We evaluate the performance of small error-correcting codes which we implement on hardware platforms of very different connectivity and coherence: On the superconducting IBM Q system One and on a spintronic quantum register consisting of a color center in diamond. Taking the hardware-specific errors and connectivity into account, we investigate the dependence of the resulting logical error rate on the platform features such as the native gates, the native connectivity, gate times and coherence times. Using a standard error model parametrized for the given hardware, we simulate the performance and benchmark these predictions with experimental results when running the code on the IBM quantum device. The results indicate that for very small codes, IBMs hexagonal layout proves advantageous, yet for larger codes the star-like connectivity of the color centers enables lower error rates.

Figures

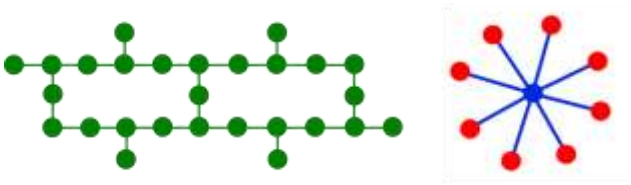

Figure 1: Quantum computing platforms of different connectivity: On the left, the coupling map of IBM Q System One is shown, while the figure on the right sketches the native connections in a spintronic system based on color centers in diamond.

References

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