Multi-level 3D device simulation approach applied to quantum-confined nanowire field effect transistors

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While electronic devices have been continuously shrunk over the past 50+ years. In the last years, this has been possible thanks to the state-of-the-art FinFETs. However, this architecture cannot provide the required electrostatic integrity when scaled to future sub 5-nm technology nodes [1]. Hence, gate-all-around nanowire (NW) FETs are considered as a replacement thanks to their superior electrostatic integrity against FinFETs and nanosheet FETs.

Modelling of semiconductor devices via technology computer-aided design (TCAD) undoubtedly plays an essential role in the scaling of transistors. TCAD tools based on quantum-mechanical corrected classical and semi-classical transport methods can provide a good trade-off between the simulation precision and computational cost. However, when studying devices with channel cross-section dimensions below 10 nm, quantum confinement starts to play a substantial role in the band-structure [2].

We present Monte Carlo simulations of NW FETs parametrized from a tight-binding calculation of the NW band structure. These simulations show that, indeed, quantum confinement effects have a big role in devices based on NWs with diameter ~<6 nm.

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References

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Figures

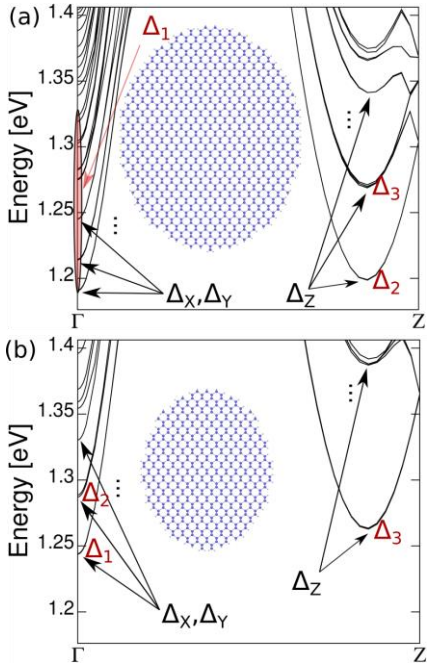

Figure 1: Tight-binding band structure of an elliptical cross-section [110] SiNW FET channel.

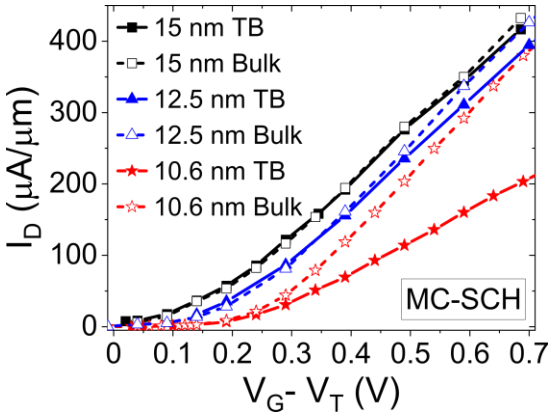

Figure 2: MC simulations of several gate length SiNW-FETs using bulk or tight-binding bands.