Hybrid classical-quantum interfaces for circuit boosts

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High-connectivity or high-depth circuits are a major roadblock for current quantum hardware. We propose hybrid classical-quantum algorithms to simulate such circuits from much shallower circuits and without swap-gate ladders. As main tool, we introduce *quantum-classical-quantum interfaces*. These cut an experimentally-problematic gate (e.g. a very long-range one) out of the circuit by random measurements and state-preparations drawn according to a classical quasi-probability simulation of the noiseless gate. As any sampling scheme based on negative quasi-probabilities, our method suffers from the infamous sign-problem. However, each interface only introduces a multiplicative statistical overhead that is independent of the on-chip qubit distance, remarkably. Hence, by applying interfaces to for instance the most long-range gates in a target circuit, significant reductions in depth (and therefore accumulated gate-infidelity) can be attained in practice. We numerically show the efficacy of our method with a Bell-state circuit for two qubits increasingly far apart on a chip, a variational ground-state solver for TF Ising model on ring lattices of increasing lengths, and with depth extensions for random circuits as well as VQEs for quantum chemistry. Our findings provide a versatile toolbox for both error-mitigation and circuit boosts tailored for noisy, intermediate-scale quantum computations.

References

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Figures

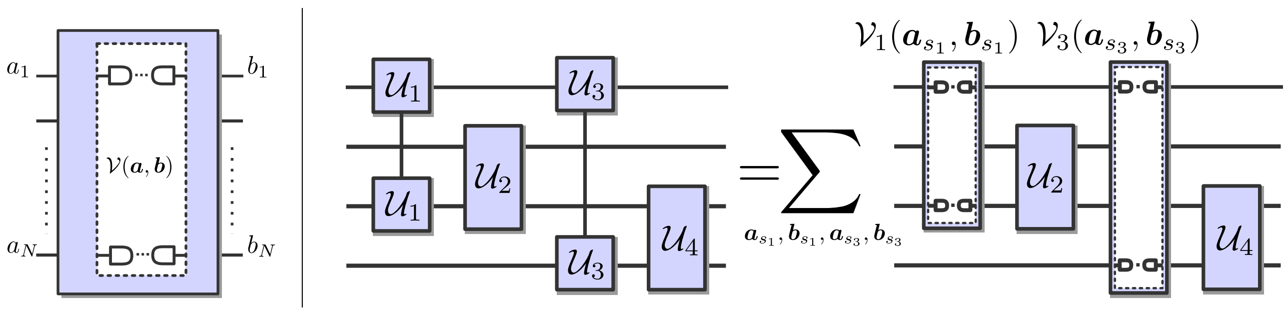

Figure 1: Schematics of our hybrid scheme. Left: A QCQ interface simulates a gate between qubits 1 and *N*. The two qubits are measured in random single-qubit bases and re-prepared in a random product state. The other *N*-2 qubits are left intact. Right: A 4-qubit high-connectivity circuit is simulated with nearest-neighbour gates without swap-gate ladders, with the long-range gates substituted by QCQ interfaces. The summation represents the average over all interface outcomes sampled. The same principle can be applied to simulate entire slices of a target circuit, leading to drastic reductions in experimental-circuit depth at the expenses of a moderate statistical overhead.