Wafer-scale graphene: a transfer-free approach

Sten Vollebregt
Delft University of Technology, Mekelweg 4, Delft, The Netherlands
s.vollebregt@tudelft.nl

Graphene has several unique properties which make it an attractive material for sensors, optoelectronics, or as nano/micro-electro-mechanical systems (NEMS/MEMS). To allow integration into semiconductor technology, graphene deposited by chemical vapour deposition (CVD) on a metal catalyst is widely regarded as the most promising method as it results in high-quality material which is required for many of the before-mentioned applications.

A downside of CVD graphene is that it requires the transfer of the graphene from the, typically, Cu, Ni, or Pt catalyst. This transfer step introduces polymer contamination, cracks, wrinkles and can result in adhesion issues with the target substrate, especially for non-flat substrates [1]. While significant progress has been made in CVD graphene and transfer [2], there still does not exist an ideal recyclable growth template and, especially, a repeatable and scaleable transfer method.

In this work, we present our wafer-scale transfer-free alternative based on Mo as catalyst which can circumvent the above-mentioned issues involved with transfer [3]. The key to this technology is the pre-patterning of the Mo catalyst layer by photolithography. Upon removal of the catalyst, the few-layer graphene adheres to the substrate at the edges of the pattern. Therefore, lithographic control over the location and size of the graphene is achieved.

By keeping the Mo underneath the graphene through post-processing to realize devices adhesion issues can be prevented. Furthermore, it enables surface and bulk micromachining allowing suspended graphene device formation on wafer-scale, fig. 1 [4]. Limitations of the technology are that the growth is coupled to the target substrate, and that - so-far - we have only been able to achieve this for few or multi-layered graphene.

Finally, we have demonstrated that our transfer-free process can also be integrated with CMOS, fig. 2 [5]. We inserted the graphene deposition step directly after the front-end of our in-house CMOS process. Care must be taken to protect the graphene layer during the back-end processing of the two-level interconnects. With this, we have demonstrated an alternative route for graphene device integration on CMOS which avoids many of the challenges related to transfer and can enable the realization of smart (suspended) graphene-based sensors.

REFERENCES

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FIGURES

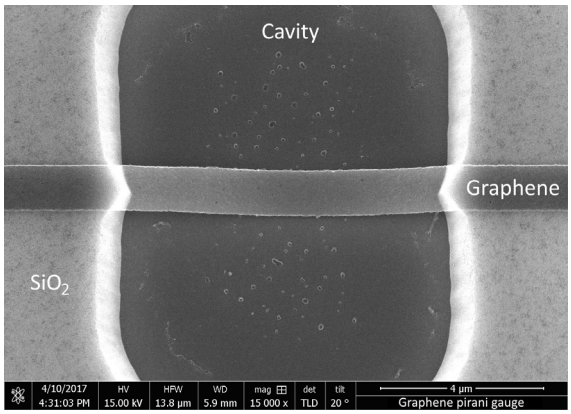

Figure 1: SEM image of a transfer-free suspended multi-layer graphene-based Pirani pressure sensor. The graphene bridge is 1 µm wide, while the SiO2 is 600 nm thick.

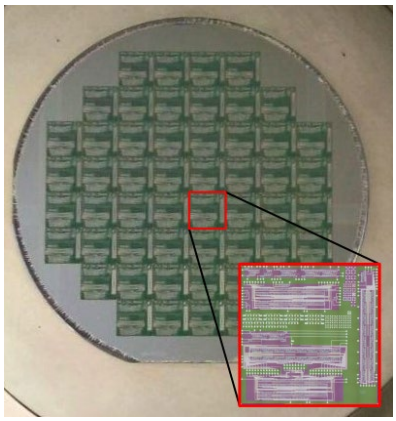

Figure 2: Wafer (10 cm) with digital CMOS circuits and transfer-free graphene integrated alongside. Both the graphene devices and CMOS circuits were found to be working.