Underlayer selection for TiSiN ALD deposition on copper thin film

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1. Introduction

In the semiconductor industry there is a major drive to integrate ALD deposition in back-end-of-line (BEOL) applications, as it comes with substantial deposition benefits, such as near perfect conformity, homogeneous film structure and composition. These characteristics enable higher compacity of integrations. TiSiN is a promising material for BEOL applications due to its good copper barrier properties [1]. However, commercially available thermal ALD process of TiSiN is slightly above 400°C. At these temperatures, exposed copper layers tend to produce surface defects, commonly known as hillocks [2]. The aim of this work is to evaluate the morphological performance of a capping layer on exposed copper before TiSiN ALD metallization: an underlayer (UL).

2. Methods

Within this work 4 stacks were evaluated: a reference and three different metal underlayer (room temperature Ta PVD / 350°C W PVD / 400°C TiN CVD) were integrated on 300mm silicon blanket wafers, between a Ta barrier + 90nm Cu PVD layer and a 12nm 440°C TiSiN tALD layer. A short airbreak tool place between depositions on each wafer. High resolution XTEM (JEOL NEOARM 200kV) was conducted to observe the interfaces.

3. Morphological analysis

The experimental results are the following, Fig. 1: (a) No UL: High copper roughness and hillock formation, no intermixing between layers, (e) TiSiN crystallinity at copper interface, segregation of elements at interface, no TiSiN oxidation on either side. (b) Ta UL: No copper roughness, no intermixing, underlayer oxidation, crystalline Ta UL, amorphous Ta(O) and TiSiN. (c) TiN UL: Medium copper roughness, (k) intermixing with copper and TiSiN, (g) crystalline TiN with an amount of intermetallic formation. (d) W UL: copper oxidation, medium copper roughness, no intermixing, slight underlayer oxidation, (h) crystalline W and amorphous TiSiN layer.

Firstly, in the Fig.1 (a), as expected, direct high temperature TiSiN deposition induces Cu roughness and even causes the formation of hillocks. Secondly, in Fig.1 (c)/(d) The 'faster' PVD and CVD in temperature only induce grain movement and local roughness, with the 'cold' Ta(N) PVD being almost perfectly flat, Fig.1 (b). Due to airbreaks most processes exhibit interface oxidation and/or degradation, apart from TiN CVD UL, which intermixes with the copper on one side, and TiSiN on the other. Here, TiSiN tends to stabilize as an amorphous layer, its crystallinity on copper is hypothesized to be caused by different stoichiometry within the first layers.

UL deposition in temperature induces slight roughness, only room temperature deposition leaves a flat copper interface. Material-wise, tantalum or tungsten are presenting good barrier morphologies, whereas TiN CVD intermixing on either side does not demonstrate real separation.

The oxidation of interfaces could be prevented by integrating a copper reduction process before UL deposition, as well as TiSiN capping without airbreak.

4. Conclusions

The interfaces between TiSiN, Copper and three underlayers were evaluated by HR XTEM. The morphological analysis exposes severe interface degradation as well as copper movement for TiSiN ALD deposition without an underlayer. Several interface defects can be observed for each above shown tested condition, with each its drawbacks. The combination of materials and process temperature indicates that a low temperature deposition of tantalum or tungsten would make an ideal underlayer.

References

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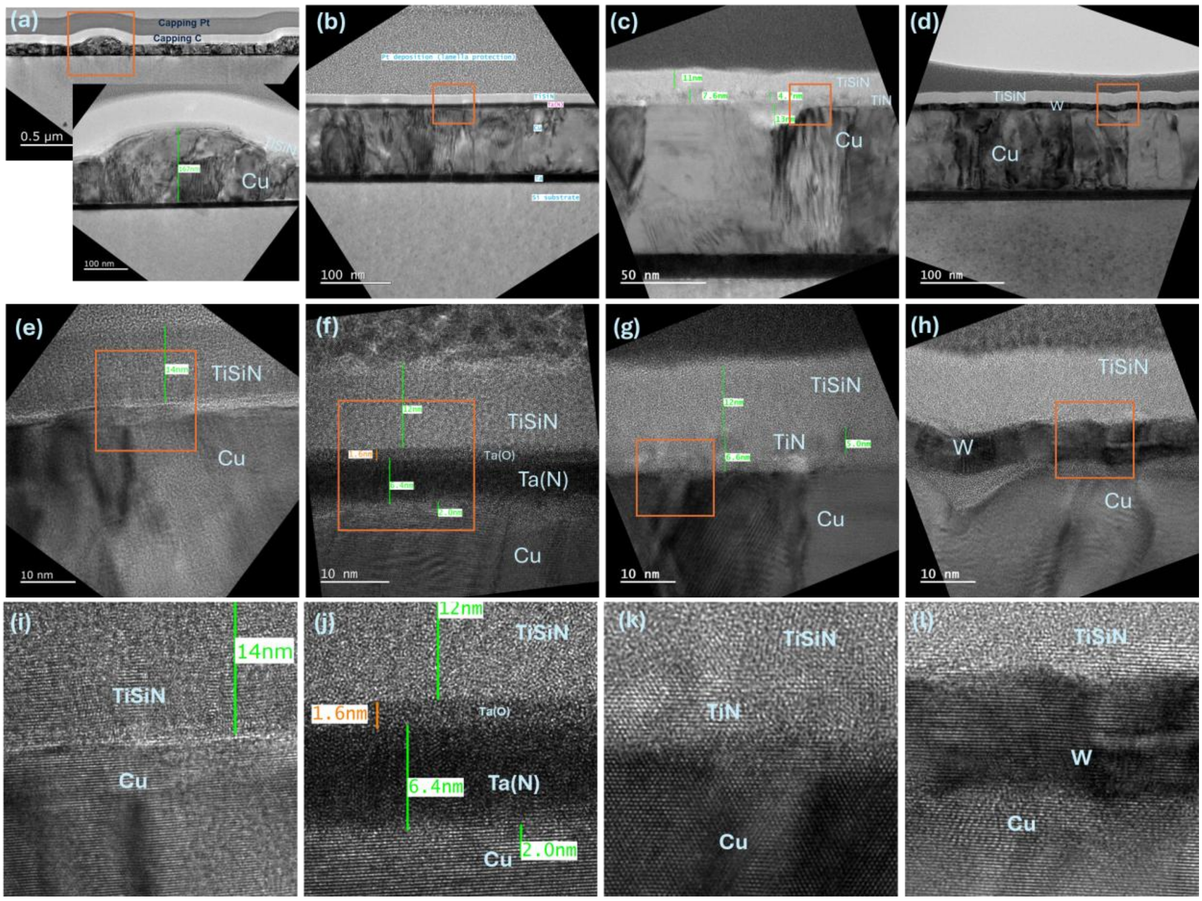

Fig. 1: Bright field high resolution TEM images of four stacks - (a)/(e)/(i) Cu PVD + TiSiN ALD – (b)/(f)/(j) Cu PVD + Ta(N) PVD + TiSiN PVD – (c)/(g)/(k) Cu PVD + TiN CVD + TiSiN ALD – (d)/(h)/(l) Cu PVD+ W PVD+ TiSiN ALD