Ruthenium Based BEOL Integration Schemes for Scaled Interconnects

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Reducing interconnect resistance and capacitance remains essential to sustain performance as BEOL scaling enters the sub-20 nm metal-pitch regime, where RC delay, variability, and integration complexity rapidly increase [1]. Direct-metal-etch ruthenium (Ru) [2-5] has emerged as the leading candidate replace copper (Cu) for the most scaled metal levels, owing to barrier-less integration, limited resistivity degradation at reduced dimensions, and superior electromigration robustness. In parallel, process options such as fully self-aligned vias (FSAV) and air-gap structures are proving effective at lowering capacitance and mitigating via-to-line leakage [4, 5].
In this invited talk, we present imec's BEOL roadmap direction and the Dual Direct Metal Etch (DDMe) [1] integration approach. DDMe enables multi-layer FSAV through direct etching of both line and via levels, removes conventional barrier/liner stacks in vias and it is highly compatible with air-gap integration. Recognizing that Cu will remain essential in upper metal levels, we also focus on on Cu/Ru co-integration. Using stacked-via resistance modelling and experiments on selective Ru (Vias) on Cu (wires) via in EUV-patterned dual-damascene levels, we show that hybrid Ru-via/Cu-wire schemes bring substantial performance benefits even though more work is needed on the integration approach compatible with DDMe [9]. Collectively, DDMe and hybrid Ru/Cu metallization constitute a flexible, manufacturable platform to address near-term RC and variability constraints while keeping optionality for future conductors and heterogeneous BEOL stacks [10, 11].

References

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