Development of a WOW-Compatible Chiplet-Based COW Process

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Chiplet-based Chip-on-Wafer (COW) technology is effective for the parallel integration of known-good dies (KGDs) and heterogeneous devices. In the post-scaling era, further increases in integration density and reductions in stacking pitch are required, while highly productive manufacturing technologies are simultaneously demanded. From a productivity perspective, wafer-level stacking using Wafer-on-Wafer (WOW) technology [1][2] offers a low-cost solution; however, conventional COW processes are not compatible with WOW interconnection and stacking processes.

In this study, we developed a novel thin-profile COW process, BBCube™ 2.5D, in which dies are bonded face-down without using bumps [3–5]. COW wafers fabricated using this process can be stacked and interconnected as WOW wafers.

The detailed fabrication procedure of BBCube 2.5D is shown in Fig. 1 and described as follows.

a. Waffle wafer formation: A 300-mm silicon wafer is patterned by dry etching to form rectangular trenches, creating a waffle-shaped structure designed to accommodate dies.
b. Adhesive coating and tack cure: A permanent adhesive is selectively coated onto the trench bottoms using an inkjet or patterned coating process. The adhesive is tack-cured prior to die placement.
c. Face-down die placement: Dies are picked, flipped, and bonded face-down into the trenches. The tack-cured adhesive suppresses die shift and tilt.
d. Molding and thinning: The wafer is molded with resin and subsequently thinned from the backside of both the dies and the waffle wafer.
e. Via-last TSV and pad formation: Through-silicon vias are etched from the backside of the waffle wafer and connected directly to the die electrodes using a BEOL-compatible via-last process. Backside redistribution layers (RDLs) are then formed to provide lateral inter-die signal routing and power distribution.
f. Device wafer stacking and TSV formation: The thinned device wafer is bonded using a thin SiOC adhesive with wafer-to-wafer alignment, followed by TSV and RDL processing afterward.
g. Dicing and singulation: The wafer is diced and singulated into individual multi-chip packages for subsequent assembly and testing.

By adopting the face-down die configuration, die thinning can be performed from the backside after die placement. Because the waffle wafer can also be thinned from the opposite side, TSV length is reduced, and adjacent dies can be interconnected through RDL-based wiring. Furthermore, the resulting COW wafer enables bumpless TSV interconnection for subsequent stacking. This work establishes a practical pathway for manufacturing chiplet-based heterogeneous systems using a bumpless WOW process.

References

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[2] T. Ohba, et al. “Review of Bumpless Build Cube (BBCube) Using Wafer-on-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI),” Electronics, 236 (11), pp. 1-57, 2022.
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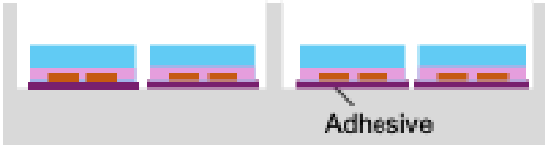
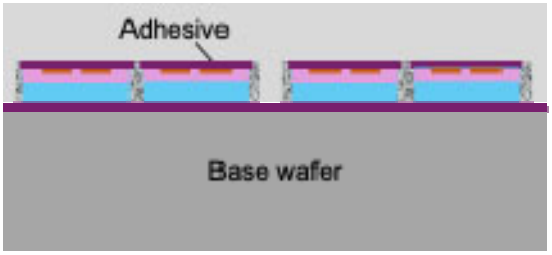
Fig. 1. Process flow of face-down bumpless COW and WOW.

a. Waffle wafer formation

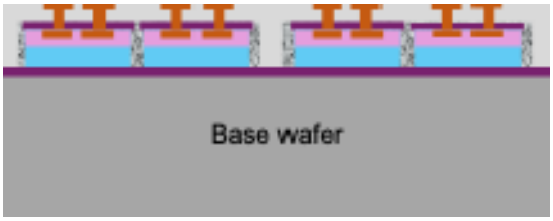
b. Adhesive coating and tack cure

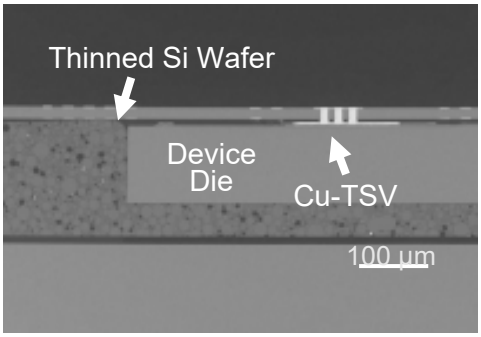


c. Face-down die placement

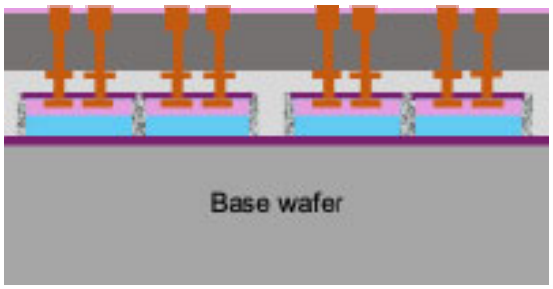


d. Molding and thinning

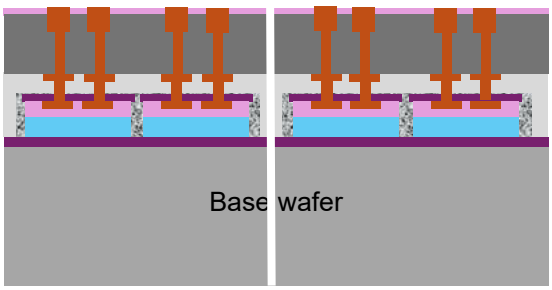




e. Via-last TSV and pad formation



f. Device wafer stacking and TSV formation



g. Dicing and singulation