Plasma enhanced Atomic Layer Etching on AlGaN/GaN: process development, stability, recess etching of source, drain and gate

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Continuous device miniaturization necessitates etching techniques with exceptional precision and control. ALE is a key process technique enables precise, controllable etching with minimizing the structural damage and therefore enables new possibilities in device manufacturing [1]. The plasma ALE process consists of two independent steps forming a repeatable cycle. In the case of AlGaN etching, the first step involves chemical surface modification, achieved through halogenation using Cl_2 plasma. In the second step, the modified surface layer is removed by low energy Ar ion bombardment [1-8]. Typically purging in between the steps is applied, which increases the cycle time and affects the processing costs, too. A high degree of self-limitation in each step determines the controllability and stability of the process. Overall, the tool condition strongly impacts the EPC and self-limitation.

Atomic Layer Etching (ALE) has become increasingly important as a precise technique for AlGaN/GaN-based device fabrication, enabling highly controlled gate or contact recess etching. By recessing the barrier below the ohmic contacts, the contact resistance can be improved, which is beneficial for the overall Ron of the AlGaN/GaN HEMTs [9] and therefore decreases the switching losses and helps to exploit the full potential of those devices. With a controllable and low-damage gate recess the threshold voltage V_{th} can be tuned and shifted even to positive values [10-15].

We will demonstrate that maintaining process reproducibility in ALE of AlGaN is challenging due to chamber wall contamination. Chlorine compounds deposited during modification steps can desorb into the argon removal plasma, disrupting self-limitation and altering EPC. Long operation can challenge chamber cleanliness and process reproducibility, making in-situ monitoring, such as optical emission spectroscopy, necessary. Chamber cleaning and conditioning procedure were established, and it will be demonstrated that they are critical for maintaining process repeatability and should be incorporated into process development.

As a second focus the cycle time was reduced to improve costs and sustainability of conventional ALE. Due to additional purging and evacuation sequences after each step, an ALE process lasts longer than a conventional reactive ion etching (RIE) process [16]. By minimizing or eliminating purge steps [16, 17] and optimizing plasma parameters or combining chemistry within one process step [18], cycle times can be reduced. For this reason, five ALE modifications were developed and compared: full-purge (1), half-purge (2), purge-free (3), continuous plasma (4) and bias pulsing (5). Their sequential structure over time is shown in Fig. 1a. Thereby the overall process time can be reduced by more than 60% while maintaining low EPC (0.2 ± 0.02) nm/cycle and low surface roughness of 0.3 nm. [19]

Finally, AlGaN/GaN HEMTs were fabricated using optimized ALE modes, which were successfully applied for gate [17] and ohmic contact recesses. A linear relationship between V_{th} and etch depth can be demonstrated (Fig. 1b). For ohmic contact recess etching an optimum for certain recess depth could be achieved with significantly reduced contact resistance (< 0.2 Ωmm) for gold-based Ti/Al/Ni/Au stacks (Fig. 2) and allowed lower annealing temperatures, reducing thermal stress and improving CMOS compatibility.

The combination of robust chamber cleaning and conditioning, rapid ALE recipes demonstrate a cost-efficient and sustainable tool to optimize the device performance of conventional lateral HEMT devices.

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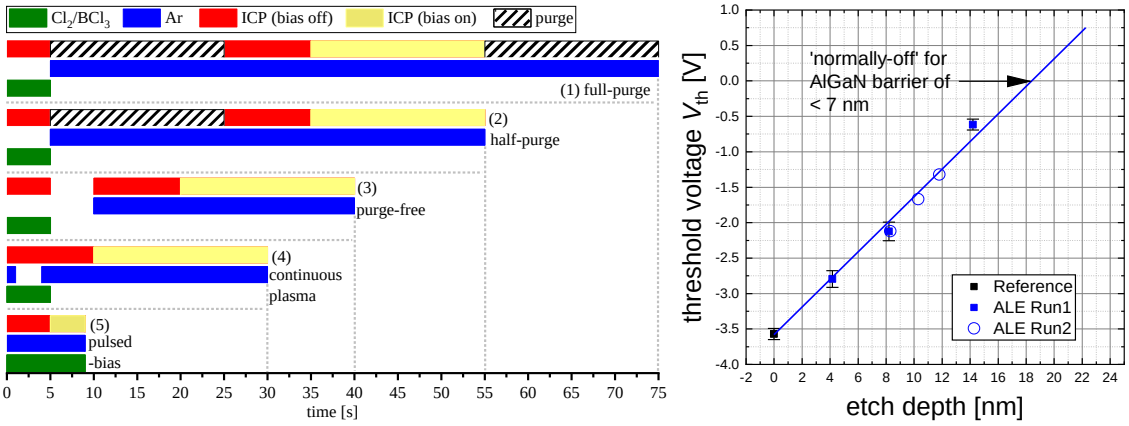

Fig 1. (a) Cycle sequence over time for the five different ALE modes. (b) Threshold voltage V_{th} extracted from step in gate capacitance. V_{th} increases linearly with etch depth.

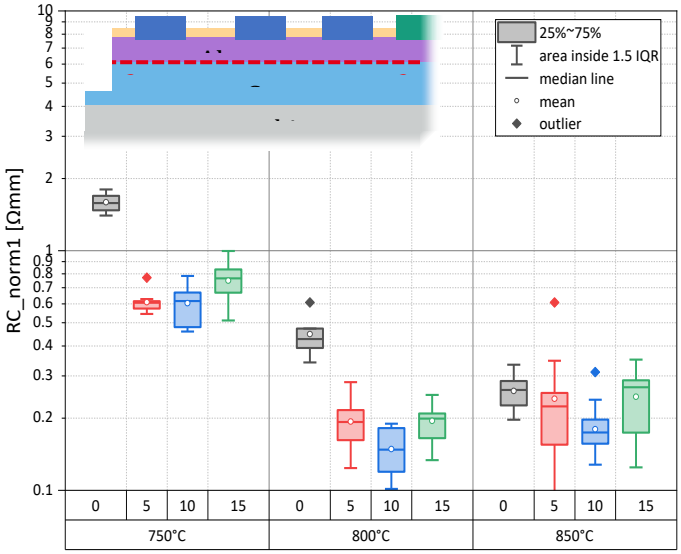

Fig 2. Results of electrical characterization of recessed ohmic contacts. Reducing the contact resistance for 750 °C, 800 °C and 850 °C annealing temperature with visible trend and optimum is achieved at 10 nm recess etch.