Co-Registered Automated Optical Inspection and Metrology for C4/TCB Micro-Bumps with Infrared Structured Illumination Microscopy of Bonded Interfaces

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C4 flip-chip and thermo-compression bonding (TCB) interconnect schemes require the simultaneous control of micro-bump geometry (e.g. height, coplanarity, critical dimensions and deformation) and defectivity (e.g. missing/partial bumps, bridges, residues, damage and process excursions). Furthermore, advanced packaging process flows necessitate in-line measurements on both full wafers and chips on film frames, accompanied by robust automation and actionable statistics on substantial sample sizes. In practice, the separation of defect inspection and metrology frequently introduces registration uncertainty and limits correlation between defect appearance and quantitative geometry.

In this paper, we present a precision optical platform in which defect inspection and 3D/2D metrology share a single optical beam path, generating inherently co-registered datasets. The concept of "what you see" being aligned with "what you measure" by design is a fundamental principle that underpins the system. The system is based on Structured Illumination Microscopy (SIM) for quantitative topography and material-independent surface measurement, supporting nanometer-scale vertical sensitivity for demanding topographies such as micro-bumps and high-aspect-ratio features [1,2]. In the context of micro-bump AOI, high-resolution imaging is combined with AI-driven workflows (e.g., classification/segmentation/anomaly detection) to minimize false positives and enhance decision-making for process optimization [3].

A key enabler for information-rich micro-bump analytics is high sampling density. With an effective pixel size down to 0.55 µm at 10× magnification, the acquired data density is 3× higher per unit area compared with respect to state-of-the-art tools. This enables more robust bump-shape descriptors, tighter coplanarity statistics, and improved sensitivity to outliers in large populations. The platform has been engineered to measure hundreds of millions of bumps per wafer, perform automated statistical analysis, and flag defective bumps while delivering both defect review imagery and full-wafer image outputs.

In the context of wafer bonding, infrared is utilised for the specific purpose of inspecting and metrology of bond-interface. The present study proposes an extension of SIM into the infrared domain through the implementation of Infrared Structured Illumination Microscopy (IR-SIM), a technique that integrates the penetration of infrared light through silicon with the optical sectioning of samples [4]. The method projects sinusoidal illumination patterns, acquires two phase-shifted images, and demodulates them to suppress out-of-focus contributions. This enables depth-resolved "optical cross-sectioning" and quantitative 3D reconstruction at the buried bonding plane. The demonstration is conducted on Si–Si bonded wafers, utilising IR-SIM imaging to visualise voids, delamination, and bonding non-uniformities at the interface. This approach affords true 3D morphology with sub-micrometre resolution while maintaining non-contact operation and eliminating the need for sample preparation.

Beyond micro-bumps and bond interfaces, the same measurement concept supports additional advanced-packaging metrology tasks such as depth, profile, and CD measurements of dicing trenches and TSVs, wafer warpage, and total thickness variation (TTV). These tasks are enabled by the platform's multi-sensor capabilities.

References

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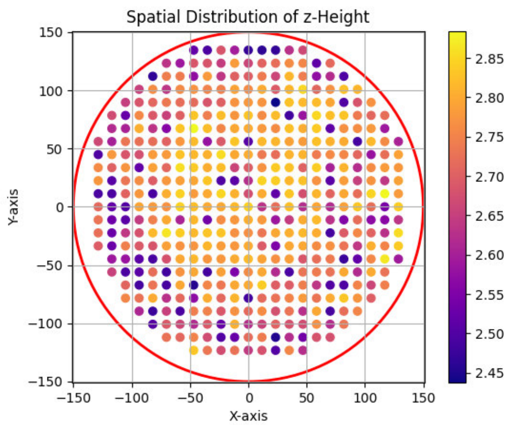

Figure 1: *Colour-coded 300 mm wafer map of the height distribution of the bumps.*

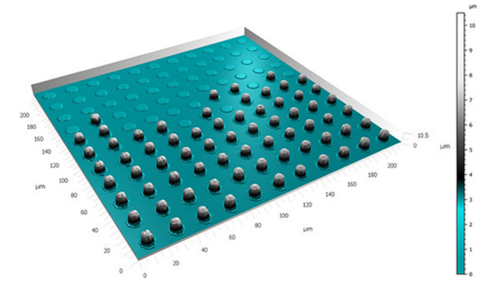

Figure 2: *3D rendering of an area with multiple missing bumps.*

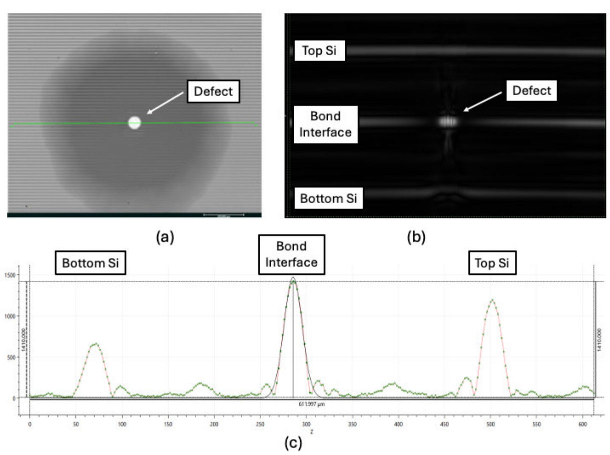

Figure 3: *(a) IR SIM top view of a defect and void at the Si-Si bond interface. (b) Cross-sectioning view of bonded Si wafers with a defect at the interface. (c) Pixel view of the wafer stack. The 3 peaks correspond to the Air-Si transition of the bottom wafer, bond interface, and Si-Air transition of the top wafer from left to right.*

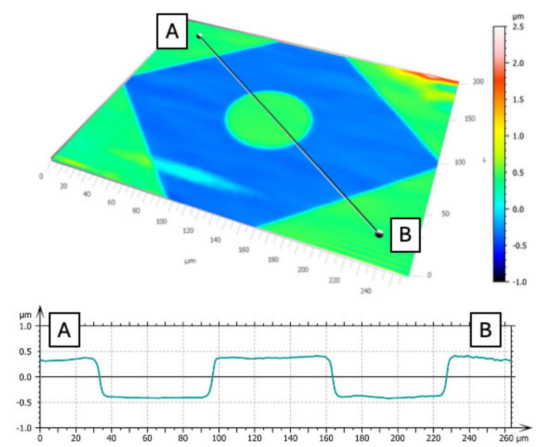

Figure 4: *(Top) 3D rendering of a square cavity with a round pillar at the bonding interface of 2 silicon wafers. (Bottom) 2D measurement of the cavity and pillar along the line A-B.*