300 mm CMOS Compatible ZrN based SC BEOL Demonstrator & Trench-Array Structures for Testing Via Superconductivity

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A superconducting back-end-of-line (SC-BEOL) is a key enabler for high-performance cryogenic electronics including Superconducting Quantum Computing control hardware and Single Flux Quantum (SFQ) digital circuits. Compared with conventional Cu BEOL technology, superconducting interconnects enable significantly higher clock frequencies while simultaneously reducing dissipative losses.

In this work, we present a 300 mm CMOS-compatible process for the fabrication of a superconducting BEOL demonstrator (Fig. 1) employing sputtered ZrN as the superconducting material and TEOS-based PECVD SiO_2 as the interlayer dielectric. The process flow is inspired by established SFQ process nodes by MIT Lincoln Laboratory [1] and imec's semi-damascene approach [2] and incorporates some non-standard integration features. First, ZrN patterning combines subtractive and additive approaches: metal layers are structured subtractively, whereas via layers are defined additively. Second, V1 and M2 are deposited within a single sputter step. As a consequence, hollow vias are formed in which ZrN is present only along the Via sidewalls.

Cryogenic four-point measurements in an OptiCool cryostat of a 2-Via structure confirm electrical connectivity through M1-V1-M2; however, the interconnects do not exhibit superconducting behavior. The absence of superconductivity is attributed either to (i) surface damage of M1 induced by the SiO_2 via etch or (ii) to a non-superconducting crystal structure of ZrN on the V1 sidewalls. For an isolated analysis of the potential influence of the altered V1 ZrN, trench-array test structures were fabricated. Arrays of 2x30 trenches with widths of 500 nm at 1:1 pitch were etched into SiO_2, followed by deposition of 50 nm ZrN (Fig. 2). For four-point measurements across the trench array, the measurement region was electrically isolated by milling a rectangular contour to a depth of approximately 200 nm using a Ga^{3+}-ion FIB (Fig. 3 & 4).
Two sample variants with trench depths of 50 nm and were evaluated at 2 K. Structures with 100 nm trench depth show purely resistive behavior below and above the critical current (Fig.5a). In contrast, the 50 nm trench depth structures exhibit superconductivity followed by a mixed regime which is characterized by resistive conduction and multiple voltage steps, and finally a transition to fully resistive behavior above the critical current (Fig.5b). The mixed regime is attributed to ZrN inhomogeneities within the trenches, causing spatially varying local critical currents and sequential loss of superconductivity.
These results indicate that geometry-dependent film properties critically influence superconducting via performance and must be tightly controlled for reliable SC-BEOL integration.

References
1. Tolpygo, S. et al., IEEE Transactions on Applied Superconductivity, Vol. 26, No. 3 (2016)
2. Pokhrel , A. et al., IEEE IITC & IEEE MAM (2023)

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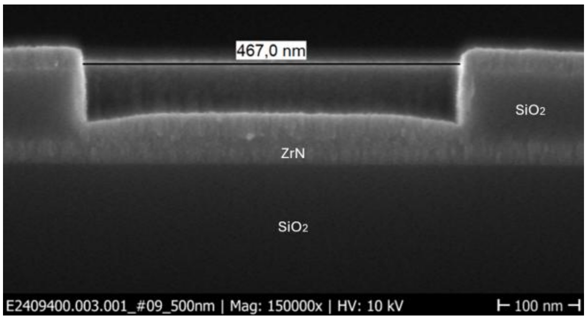

Fig.1: SEM X-Section of a ZrN based SC BEOL demonstrator with 100 nm etch depth.

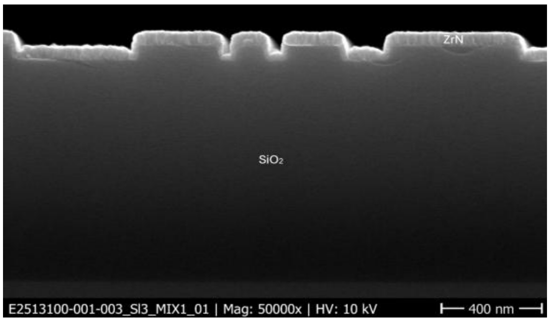

Fig.2: SEM X-Section of SEM-Bars of varying width and 50 nm etch depth.

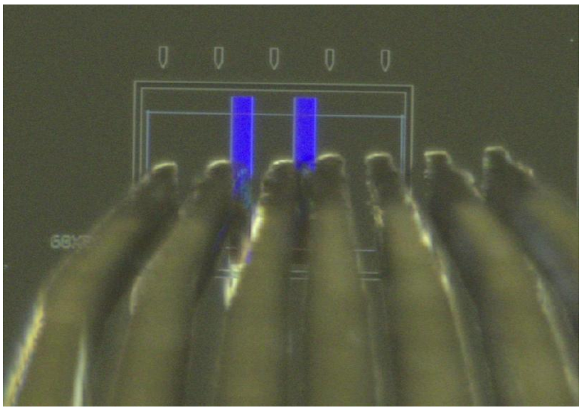

Fig.3: Four-point trench-array measurement setup with electrically isolated measurement area. The 2 × 30 trenches are identifiable by the blue coloration. The central probe is configured such that no current flows through it (I = 0 A).

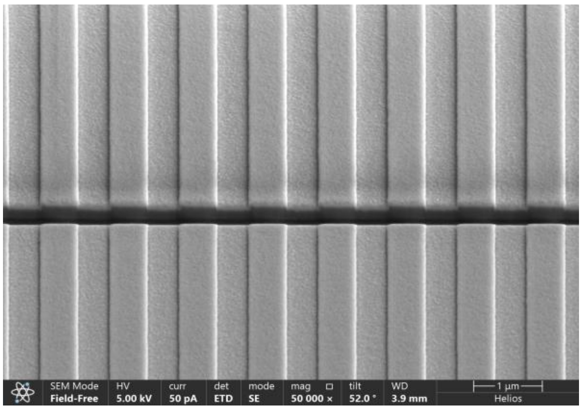

Fig.4: SEM micrograph of a 500 nm wide trench-array isolation cut produced by Ga^{3+}-ion FIB milling.

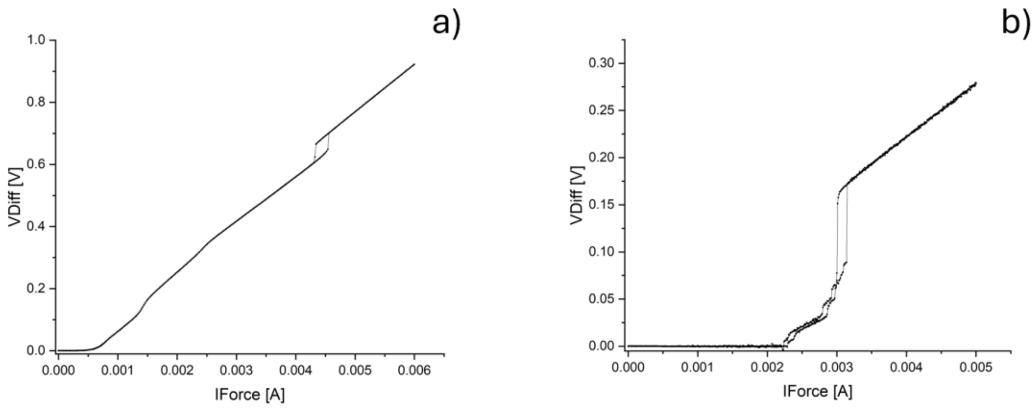

Fig.5: Four-point-IV-measurements of trench-array test structures with 500nm width at 1:1 pitch: a) 100 nm trench etch depth, b) 50 nm trench etch depth. IForce is swept in both directions.