Low-temperature formation of ultra-thin Co disilicide ($CoSi_2$) layers for advanced CMOS applications

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The transition from 4G to 5G in the coming years will enable new forms of the Internet of Things, notably the broader deployment of autonomous vehicles. This therefore requires the development of new microelectronic circuits based on MOS-type transistors (Metal Oxide Semiconductor) with gate widths of 65 nm and below. Silicides are intermetallic layers formed during annealing by reactive diffusion between a metal (Ni, Co, Ti, W, etc.) and silicon in order to be used at transistors contacts [1]. The formation of silicides helps to reduce the contacts resistance of the transistor gate, which is inversely proportional to the maximum frequency of the devices. However, for advanced CMOS technologies (gate width < 65 nm), problems arise in the formation of $CoSi_2$ (the least resistive phase) at the transistor gate. Indeed, the formation of $CoSi_2$ is preceded by the formation of the intermediate CoSi phase by reactive diffusion at a lower temperature. The $CoSi_2$ phase growth is controlled by nucleation at the triple junctions of the CoSi phase. Consequently, the downscaling of gate dimensions reduces the number of nucleation sites to form $CoSi_2$, hence narrow line effect occurs (Fig. 1) [2]. Moreover, when the gate dimension is reduced, the junction depth is also minimized to control the junction silicon consumption. The maximum of silicide thickness downs to 20 nm, inducing severe degradation of thermal stability i.e. agglomeration phenomena at a certain temperature [3].

In the present paper, the silicide layers are formed though the SALICIDE (SelfAligned saLICIDE) process (Fig. 2). It can be summarized in five principal steps: Surface preparation, Co – TiN metal deposition, RTA1 (rapid thermal annealing 1), selective etch of non-reacted metal and RTA2 step to form $CoSi_2$. For 7 nm Co, 23 nm $CoSi_2$ is expected after a total reaction of the metal. Since the thickness of $CoSi_2$ is directly proportional to the thickness of CoSi, it is possible to obtain a thinner $CoSi_2$ layer by reducing the RTA1 temperature to form less CoSi. This is called partial silicidation or partial reaction. As we wanted to reduce the $CoSi_2$ thickness, RTA1 temperature was reduced in the range of 400 °C to 500 °C. The RTA2 temperature used is 790 °C. As shown in Fig. 3, for RTA1 temperature up to 460 °C, partial reaction occurs (Co is not fully consumed during silicidation). Beyond this temperature, the reaction is total (Co is fully consumed). At the same time, the sheet resistance increases for thinner layers (Fig. 4). The TEM/EDX images show the non-continuity of the thinner silicide layers: the layers are agglomerated (Fig. 5).

To assess the influence of RTA2 temperature, several RTA1 temperatures (RTA1 410 °C, 440 °C, and 500 °C) have been kept for further studies. For RTA1 at 410 °C, the $CoSi_2$ thickness remains constant at around 12 nm in the range of 585 °C and 790 °C of RTA2 temperature. The CoSi layer is fully transformed into $CoSi_2$ even at the lowest RTA2 temperature (585 °C). For RTA1 at 440 °C and 500 °C, the $CoSi_2$ thickness evolves with RTA2 temperature, indicating that CoSi continues to be transformed into $CoSi_2$ during the annealing treatments (Fig. 6). For all RTA1 temperatures, the sheet resistance is very high at low RTA2 temperatures and then stabilizes from an RTA2 temperature of about 615 °C (Fig. 7). In fact, TEM/EDX images reveal a bilayer structure of approximately 7 nm CoSi / 10 nm $CoSi_2$ for RTA1 440 °C and 500 °C (Fig. 8).

In the full paper, we will present TEM-EDX and HR-SEM observations to evaluate the formation and the thermal stability of ultra-thin $CoSi_2$ layers in the frame of advanced CMOS technologies.

References

[1] Mangelinck, Dominique. "The growth of silicides and germanides." *Handbook of Solid State Diffusion, Volume 2*. Elsevier, 2017. 379-446.

[2] Gregoire, M. "Silicides in microelectronics: phase sequence nanoscale effect and degradation mechanisms." *Postdoctoral Thesis, Aix-Marseille Universite* (2021).

[3] Anak, Fabriziofranco Morris, et al. "Influence of the annealing schemes on the formation and stability of Ni (Pt) Si thin films: Partial, laser, total, and one-step *annealings*." *Materials Science in Semiconductor Processing* 184 (2024)

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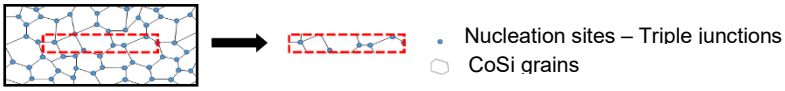

Fig. 1: CoSi grains and $CoSi_2$ nucleation sites (triples junctions)

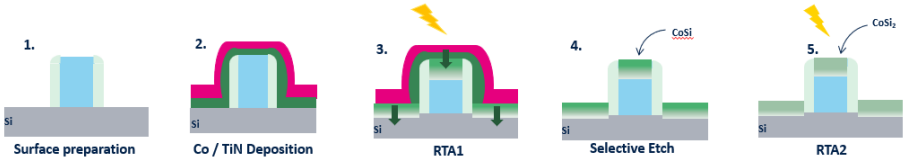

Fig. 2: $CoSi_2$ SALICIDE process

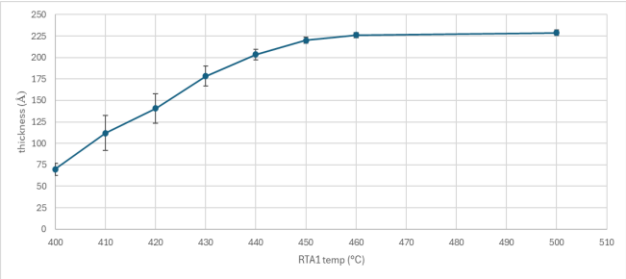

Fig. 3: $CoSi_2$ Thickness vs RTA1 temperature

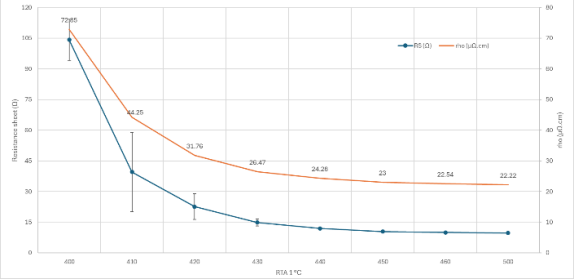

Fig. 4: Sheet resistance Rs and resistivity rho vs RTA1 temperature

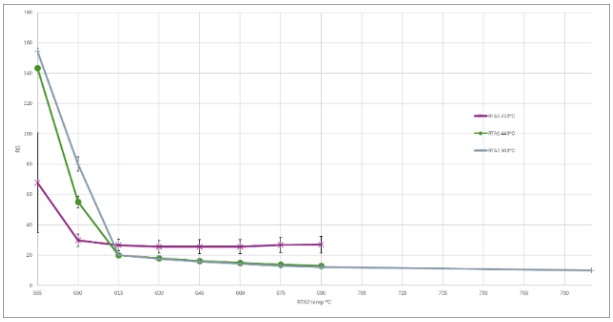

Fig 5: TEM image of agglomerated $CoSi_2$ layer corresponding to RTA1 400 °C

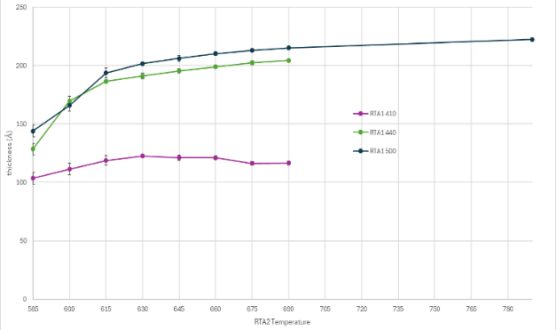

Fig. 6: $CoSi_2$ Thickness vs RTA2 temperature for RTA1 400 °C, 440 °C and 500 °C

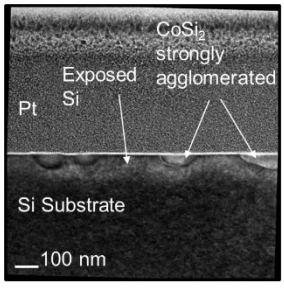

Fig. 7: $CoSi_2$ sheet resistance Rs vs RTA2 temperature for RTA1 400 °C, 440 °C and

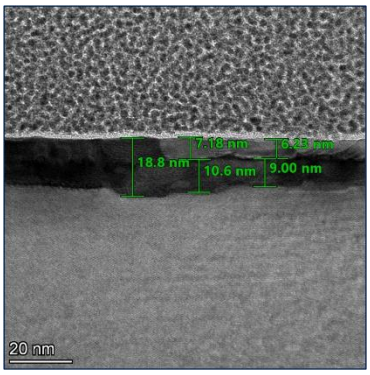

Fig 8: TEM image of ~ 7 nm CoSi / 10 nm $CoSi_2$ for RTA1 at 440 °C and