

Monitoring-Based Control and Process Interruptions Recovery Strategies for Slurry Residues in Serial CMP of IMD Oxides

Matteo Gullo, Nicholas Dalla Vedova

STMicroelectronics, Via Camillo Olivetti, 2, Agrate Brianza, Monza, Italy

In advanced integrated circuit manufacturing with AlCu metal interconnects, the planarization of intermetal dielectric (IMD) oxides by serial CMP plays a critical role in determining final surface defectivity¹. This defectivity directly impacts plug patterning quality, the adhesion of subsequent dielectric and metal layers, and ultimately device yield and reliability. Among the different process parameters, the choice of slurry can have a significant influence.

This work investigates a CMP scheme based on an elongated colloidal silica slurry containing 16% wt. dispersed particles, focusing on a specific defect type: slurry residues. The study is built around two main axes.

The first is the analysis of the impact of process interruptions within the serial CMP sequence on final surface defectivity, with particular reference to slurry residues on the oxide surface. Critical process steps and associated wait times were identified, beyond which slurry particles dry on the oxide surface. It was found that, once these critical times are exceeded under specific conditions, the resulting residues can no longer be completely removed by the subsequent cleaning step when the cleaning chemistry does not include diluted HF₂.

The second axis concerns mitigation strategies. A monitoring and alarm system was developed to detect when the critical time window is reached or exceeded, together with a dedicated recovery procedure designed to restore surface quality at the end of the process, even in the presence of such interruptions.

The combined implementation of critical-time interception and the recovery flow enables the IMD surface to be maintained within planarity and cleanliness specifications compatible with robust plug definition and good adhesion of subsequent layers, thereby minimizing the impact on device yield and long-term reliability.

References

1. Chi-Fa Lin et al 1999 J. Electrochem. Soc. 146 1984, "Process Optimization and Integration for Silicon Oxide Intermetal Dielectric Planarized by Chemical Mechanical Polish".
2. Jihoon Seo, Advances in Chemical Mechanical Planarization (CMP) (Second Edition), "18 - Challenges and solutions for post-CMP cleaning at device and interconnect levels", pages 503-532.

* corresponding author e-mail: matteo.gullo@st.com



Figure 1. Optical image of a slurry residue. Silica nano particles are visible on the surface

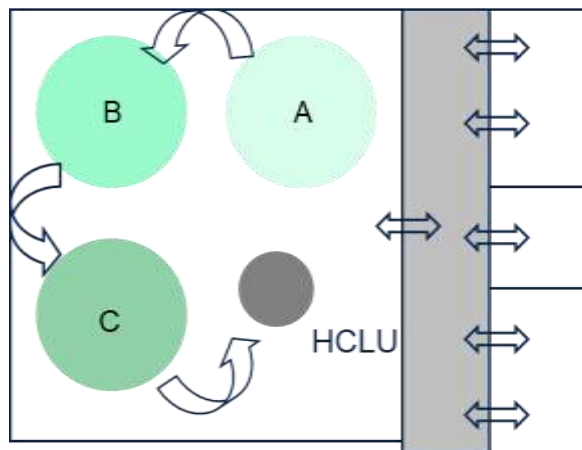
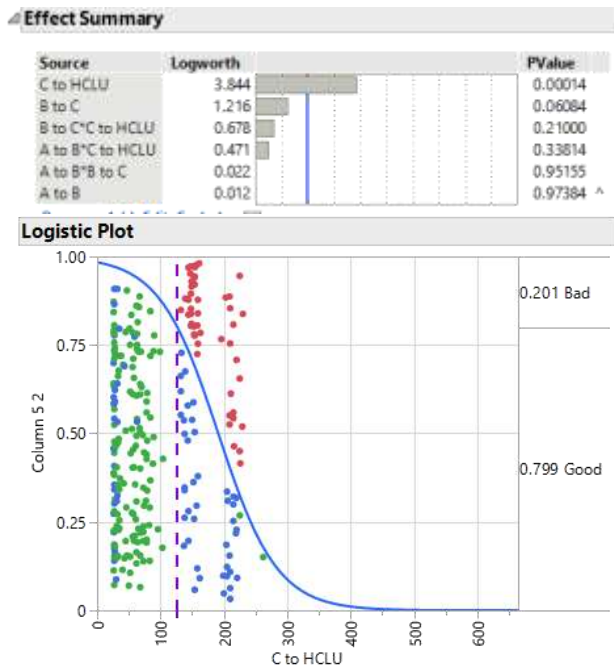


Figure 2. Serial CMP equipment scheme



Bad ← **Bad** → from defectivity check
Good ← **Good** → from defectivity check
Good (bad lot) → clean wafers from impacted lots

Figure 3. Logistic plot and Summary Effect to correlate the main contributor on the critical waiting time during CMP process with defectivity results