Chip-on-Wafer Integration Technology for Silicon Capacitor Embedded 3D Functional Interposer

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In case of the conventional 2.5D package, a large area for the capacitors is required and the wiring length from MPUs to the capacitors is long such as 5 mm. If capacitor chips are placed underneath MPUs, a shorter interconnect length between MPUs and the capacitors can be achieved. In our research, we have addressed barriers across multiple domains, including equipment and materials, to realize 3D integration technology for enhanced performance [1]. This paper describes Chip-on-Wafer (COW) integration applied to a miniaturized, capacitor-embedded 3D functional interposer.

The capacitor-embedded 3D functional interposer is fabricated by COW process on a 300 mm wafer, ensuring compatibility with Cu Damascene interconnect technology. COW process flow is shown in Fig. 1 [2]. The COW process mainly consists of three key technologies: (1) wafer warpage control utilizing waffle wafer, (2) narrow-gap chip bonding with a thin adhesive, and (3) TSV interconnects between capacitor and RDLs.

In this paper, wafer warpage control utilizing waffle wafer is focused. Wafer warpage, due to a mismatch in the CTE between Si and organic materials such as mold resin, causes wafer cracking and even wafer breakage in the worst case. To reduce wafer warpage, waffle wafer was introduced in the COW process. Waffle wafer can reduce the volume of mold resin, so wafer warpage is smaller than that of a mirror wafer.

By utilizing COW integration, capacitor embedded 3D functional interposer was demonstrated. Fig. 2 shows the parasitic capacitance as a function of interconnect length of TSV or line length for conventional 2.5 and new 3D functional interposer [3]. Since the interconnect length was reduced to less than 1/100, the parasitic capacitance was significantly reduced to 1/150 of that of conventional 2.5D. The capacitance measured in this study is as low as 50 ~ 100 fF, including TSV and RDLs. This extreme reduction of the parasitic capacitance is applicable for the low-voltage (Vdd) and lower-noise power supplies of MPUs. The COW-based capacitor-embedded 3D functional interposer demonstrated in this study integrates both capacitors and active devices, enabling further extension to high-density heterogeneous integration in advanced 2.5D/3D architectures.

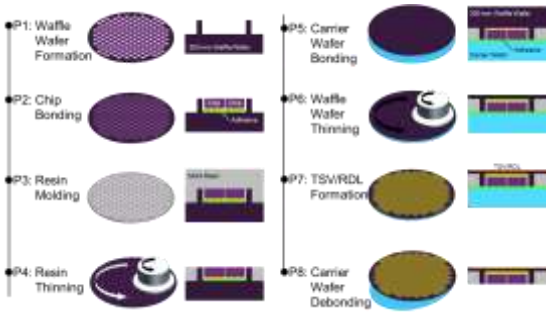

Fig. 1 Process flow for capacitor embedded 3D functional interposer are prepared using the bonding-first and TSV-last COW process.

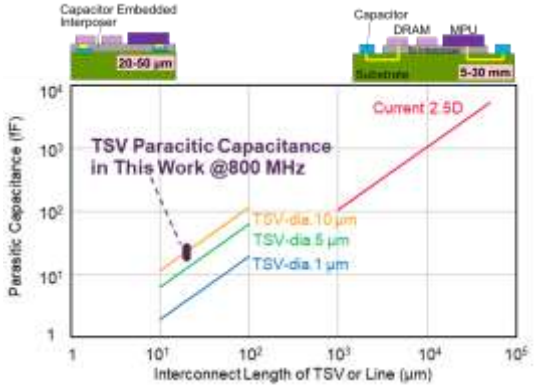

Fig. 2 Relationship between parasitic capacitance and interconnect length of TSV or line length. The interconnect length is over 5 mm in case of current 2.5D. In case that capacitor is placed underneath the active chip, the interconnect length is shortened to 20 μm.

References

1. N. Maeda, H. Kitada1, K. Fujimoto, K. Suzuki, T. Nakamura, and T. Ohba, Proc. Advanced Metallization Conf. 2008, Eds. M. Naik, R. Shaviv, T. Yoda, and K. Ueno, Mat. Res. Soc., 501 (2009).
2. T. Funaki, Y. Satake, K. Kobinata, C.C. Hsiao, H. Matsuno, S. Abe, Y. Kim, T. Ohba, 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), (2021).
3. K. Kobinata, T. Funaki, Y. Satake, H. Matsuno, S. Hidaka, S. Abe, H. Ito, C-C Hsiao, S. Y. Li, Y. S. Kim and T. Ohba, IEEE VLSI Symp., T12-3, pp. 385-386 (2022).

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