Key building blocks driving the developments of FD-SOI 10nm node

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In the context of 10 nm FD-SOI technology development, novel architectural features and process modules must be implemented to achieve the targeted device performance specifications. Strain engineering remains a key performance enabler and can be introduced either at the wafer level or locally at the device level. Additional process optimizations are required to further reduce access resistance and improve overall device characteristics. In particular, the integration of in situ doped, faceted raised source and drain regions is essential to minimize parasitic resistance. Meeting the aggressive contacted poly pitch (CPP) target of 68 nm requires the adoption of advanced patterning strategies, notably Self-Aligned Double Patterning (SADP), in order to satisfy density scaling constraints. This presentation highlights these technological levers and evaluates their impact on extending the performance capabilities of FD-SOI technology.