Wafer level technologies for Heterointegration of Photonics Modules

Stéphane Bernabé[a], Thierry Mourier,[a] , Jean Charbonnier [a]

[a] *Univ. Grenoble Alpes, CEA, LETI, Minatec Campus, F-38000 Grenoble, France*

Silicon Photonics is a key technology for Photonics / Electronics convergence. Today, increasing bandwidth needed in data center interconnects drive the deployment of silicon based advanced modules, e.g. Co-packaged Optics modules (CPO). This new paradigm strongly relies on advanced packaging technologies initially developed for memories or high-end CPUs. These wafer level technologies, such as TSVs, fine pitch interconnects of Fanout Wafer Level Packaging (FOWLP), are currently being applied to Photonic Integrated Circuits (PICs) to cope with the emerging needs, enabling volume manufacturing of high speed photonic transceivers [1].
In this presentation, we will review recent requirements related to CPOs and integrated process flows developed at CEA-LETI in order to apply such advanced packaging technologies to PIC, in various applications fields such as Optical Phased arrays (OPAs) for LIDARs, and Optical Network On Chip (ONoC) based photonic interposers for High Performance Computing (HPC).

First development has been led in order to build multi processors ONoCs. For this purpose, we developed a full integrated flow enabling TSV and wiring formation on PICs [2]. We investigated the potential influence of TSV close to optical features (such as waveguides or Ring Resonators). In some cases, influence of TSV due to mechanical stress can be observed, especially on phase-based devices (e.g. Mach Zehnder interferometers) [3]. These measurements led to establish design rules, particularly Keep Out Zones (KOZ) for future designs of complex interposers.

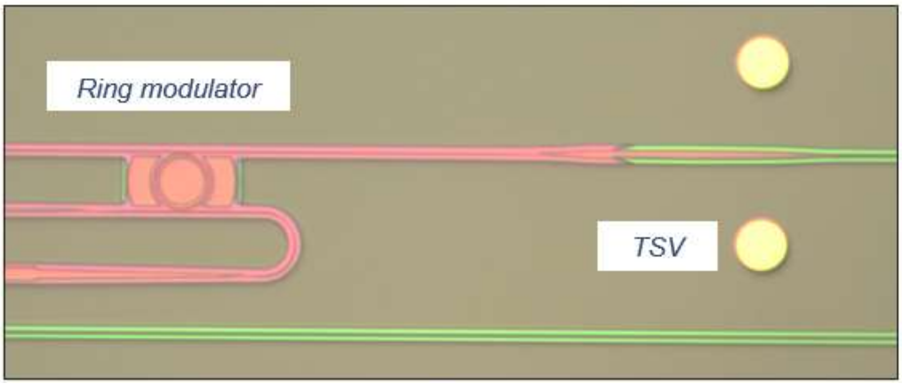

Fig 1 Top view of a photonic interposer with Ring Resonator Modulators and TSVs.

Figure 1 shows a picture of photonic circuitry integrated with TSV-mid features, used to demonstrate Optical Network On chip combining CMOS manycores chiplets, Electronic IC (EIC) dedicated to photonic devices driving and thermal management, both being flip-chip assembled on a large PIC interposer using 40µm pitch copper pillars. In [4] we recently demonstrated for the first time such an architecture with dynamic routing between chiplets, achieving the lowest published latency for a reach of around 2.5cm, while being capable of longer reach on interposer and extension to other dies through optical fiber.

In another development, we applied this mid process TSV integrated flow to OPA, in order to perform beam steering for LIDARs. Traditional wire bonding technologies lead to chips that are too large, due to the number of electrical functions to be wired, in particular the heaters used as phase shifters in the OPA. By applying our process to OPA-type photonic chips, we obtained functional demonstrators, a cross-section of which is shown in Figure 2.

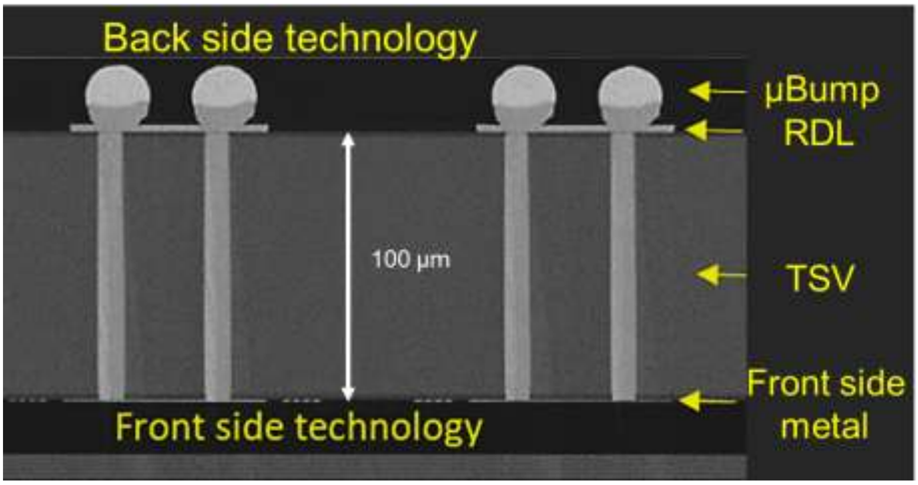

Fig 2 : Lidar OPA built using mid process TSV integration to enable back side interconnections

In this work, obtained within the TINKER European project (H2020), we performed the complete functional demonstration of our functional device, including TSV formation, chip thinning, flip-chip bonding, PCB integration and fiber pigtailing [5]. A motherboard to control the 256 channels heating, the 1550 nm laser and its power supply as well as a temperature monitoring unit have been installed in the demonstrator body and a specific software has been developed to control the different parameters of the system and generate the beam steering scenarios for the characterizations and the real time demonstration. This demonstration confirmed the validity of this approach in term of form factor and potential for collective manufacturing using standard microelectronic processes.

In order to address the requirements of coming CPO modules, several challenges remain. Among them, it is needed to develop detachable connectors to connect the PIC to external fiber optics bundles. Legacy technologies such as conventional assembly of Fiber Array Units are limited in terms of fabrication throughput and reliability. Alternative solutions rely on lensed optical schemes, relaxing the assembly tolerances of lensed connector versus lensed PICs. In this case, the placement of lenses towards PICs and fiber need to be carefully controlled. We developed several approaches, including use of self-assembly techniques relying on solder melting [6] or greyscale lithography [7].

References

1. J. Charbonnier et al, IEEE Trans. Compon. Packag. Manufact. Tech., **15,** 8 (2025)
2. D. Saint-Patrice et al., IEEE 73rd Electronic Components and Technology Conference (ECTC), p. 5-12, (2023)
3. J. Charbonnier et al., Proc. - Eur. Microelectron. Packag. Conf. Exhib., EMPC, (2025)
4. Y. Thonnart, Proc. ISSCC (2026)
5. T. Mourier et al., IEEE 75th Electronic Components and Technology Conference (ECTC),582-589 (2025)
6. T. Mourier et al., IEEE 73rd Electronic Components and Technology Conference (ECTC), 239-246 (2023)
7. O. Castany, Patent EP4102273 (2021)

* *corresponding author e-mail: stephane.bernabe@cea.fr*