Ti metallization for p-GaAsSb base contact

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Antimony Sb-based optoelectronic devices have recently attracted significant attention for their potential in lower-power, high speed electronic applications [1][2]. Among these, InP/GaAsSb double-heterojunction bipolar transistors DHBTs stand out as particularly the most interesting devices. Designed to overcome the electron blocking effect commonly observed at the base-collector heterojunction of type- I InGaAs- based DHBTs [3], these InP/GaAsSb- based type- II devices offer improved carrier transport and enhanced breakdown characteristics [4]. As a result, they have emerged as strong candidates for terahertz (THz) integrated circuit applications, achieving maximum oscillation frequencies f_{max} exceeding 1.2 THz and common-emitter breakdown voltages greater than 5.4 V.

GaAsSb layers are often metallized using noble metal such as gold, palladium, or platinum [5]. While unreacted stacks based on these metals can provide very low specific contact resistivity ρ_c, typically between 10^{-6} and 10^{-8} ohm.cm^2, they are incompatible with standard silicon fabrication lines, making them unsuitable for CMOS-compatible processes. Recently, significant progress has been made in this direction through the development of a fully CMOS compatible contact technology [6]. Alternatively, titanium (Ti) has been shown to achieve similarly low ρ_c values when deposited directly on p-GaAsSb. Its CMOS compatibility makes Ti a promising candidate for integrating III-V layers with silicon, combining low-resistance contacts with process compatibility [7]. This work spans all critical stages, including surface preparation, solid-state reaction analysis, electrical characterization, and integration strategy development, ensuring compatibility with advanced industrial processes.

The experimental protocol consists of a metallization process carried out for physicochemical characterization and the fabrication of TLM. The metallization schemes investigated in this work were based on Ti 10 nm/TiN 8 nm multilayer structures, with Ti serving both as an adhesion layer and the primary ohmic contact with the semiconductor. TiN diffusion barrier layer was used to limit interactions with ambient air. For each sample annealed with a 60 seconds RTA under N_2, average values of specific contact resistivity are shown in figure. 1.a The as-deposited sample exhibits a specific contact resistivity of ρ_c = 1.4 x 10^{-4} ohm.cm², which decreases to a minimum of ρ_c = 2.6 x 10^{-5} ohm.cm^2 after RTA at 350 °C, indicating improved ohmic contact quality. The contact resistivity remains stable up to 400 °C suggesting good thermal stability and preserved semiconductor integrity, with no significant metal diffusion or contamination. Standard deviation of ρ_c decreases significantly with temperature increasing. Beyond 400 °C a sharp increase in resistivity is observed, reaching ρ_c =2.3 x 10^{-2} ohm.cm^2 at 500 °C, indicating a loss of ohmic behavior likely caused by metal diffusion and the formation of interfacial compounds.

In order to further improve ρ_c for the lift-off flow, an additional thermal treatment was performed in two successive steps: 60 seconds at 250°C, followed by 60 seconds at either 450°C or 500°C. The results in figure 1.b shows that two successive annealing steps allows that Ti (10nm) / TiN (8nm) stack remains stable up to 450 °C, with a specific contact resistivity optimized at ρ_c =2 x 10^{-5} ohm.cm^2. Beyond this temperature, irreversible degradations occur, affecting both the metal interfaces and the semiconductor.

To further investigate these Ti-based contacts, ToFSIMS analysis was performed on the TiN/Ti/GaAsSb system right after metal deposition and after annealing at 300 °C, 400°C and 500°C (see Fig. 2). The measurements were conducted in positive polarity to effectively monitor the system evolution. A clear interface is observed without annealing between Ti and GaAsSb layers even if oxygen signal shows a low intensity due to native oxide presence on the top of III/V surface before the metal deposition. After 300°C annealing, Ga element begins to diffuse in Ti layer leading to the onset of $TiGa_x$ intermetallic alloy formation at the Ti/GaAsSb interface. At 400°C, the Ti layer becomes significantly thinner while $TiGa_x$ grows, evidencing a stronger reaction at the interface. At 500°C, the Ti layer is almost fully consumed, and a mixed region containing Ti, As, and Sb is detected at Ti /GaAsSb interface, confirming advanced chemical reactions between the metal and the semiconductor.

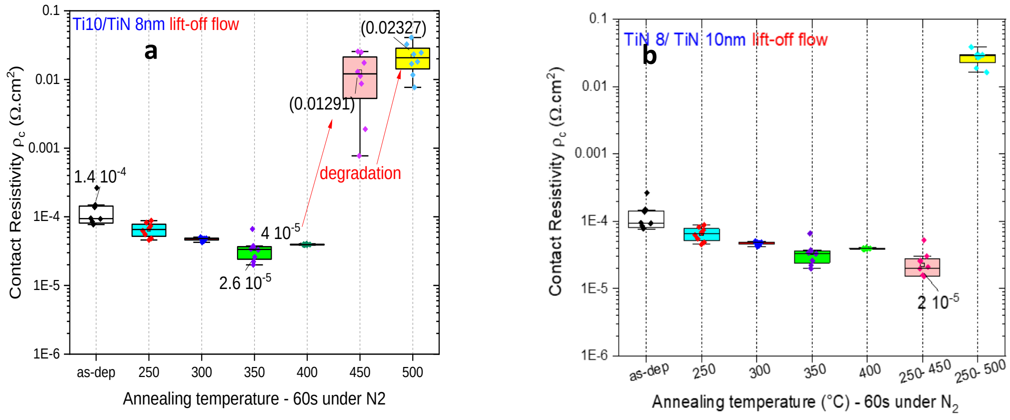

***Fig. 1 .a .b –** Specific contact resistivity of the Ti (10nm) / TiN (8 nm) stack on carbon-doped GaAsSb as a function of temperature .*

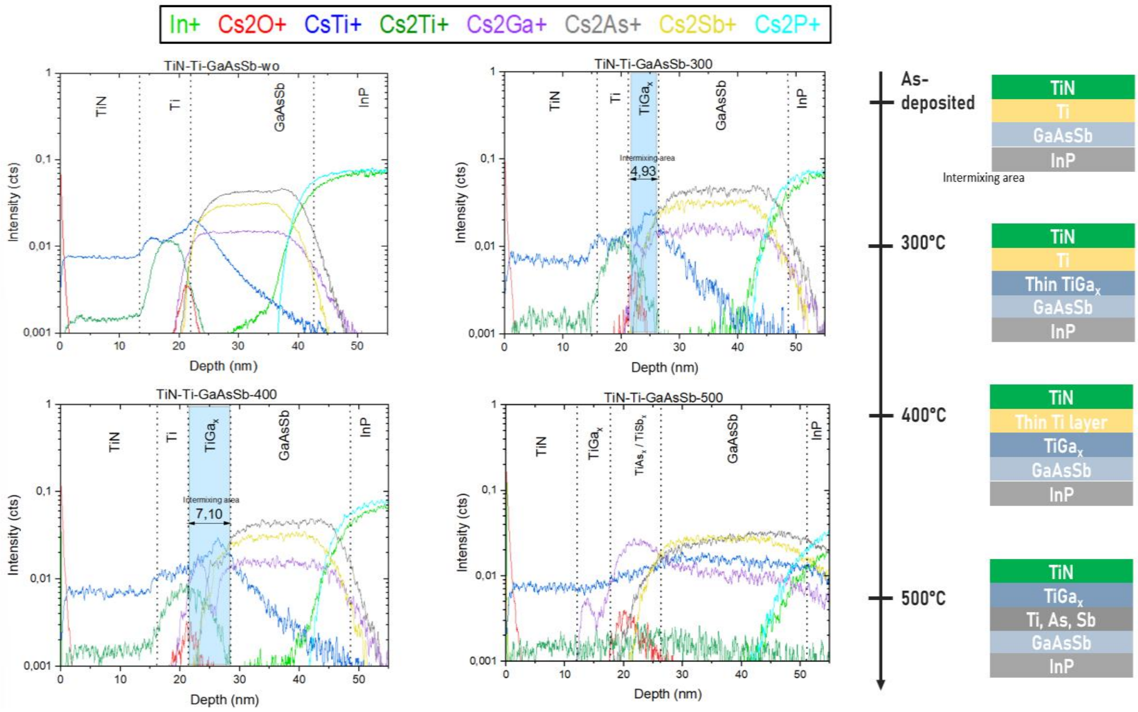

Fig.2 – T*oFSIMS profiles of the TiN/Ti/GaAsSb system annealed at various RTA*

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