Analytical evaluation of the interface states on SiO_2/4H-SiC n-type MOS Capacitor

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The increasing adoption of silicon carbide (SiC) in power devices is justified by its superior properties compared to the already established and widely used silicon (Si). The ability to operate at high temperatures and its high breakdown voltage make it a key material in the transition to systems requiring high efficiency and high power [1]. Although several generations of SiC devices are commercially available today, this technology is far from mature.

Indeed, the metal-oxide-semiconductor (MOS) interface of SiC, a critical component in MOSFET devices, still demands extensive investigation compared to Si. The interface traps (D_{it}) formed during device manufacturing are significantly higher in SiC-MOSFETs than in their silicon counterparts [2]. These traps affect the channel mobility, threshold voltage, and reliability, ultimately impacting the electrical properties of the device [3]. Understanding the influence of oxide/semiconductor interface traps on channel activation is therefore essential for advancing SiC-based MOSFETs. The high D_{it} in SiC remains a key challenge, as it leads to variations in channel mobility and compromises the device's final electrical performance.

To determine the impact of those traps on the activation of the device and, consequently, on the capacitance-voltage (C-V) characteristic curve of the MOS region in the gate of a MOSFET, the analysis was limited to the MOS interface, using a MOS capacitor as an approximation. An analytical approach was employed without the use of TCAD simulators, taking as reference a nitrogen doped n-type MOS capacitor with a semiconductor doping concentration of $7.8 \cdot 10^{15}\,cm^{-3}$, a silicon oxide layer with a thickness of 45 nm and a metal with a work function of 4.05 eV relative to the vacuum energy level. This value corresponds to the typical poly-Si work function used in MOSFETs. The advantage of using a metallic contact with a specific work function is that it eliminates potential depletion effects of poly-Si, which can appear in the C-V curve of the device in the inversion region, allowing the focus of the study to remain solely on the effects of interface traps.

A detailed analytical model that include distributed and discrete interface levels will be presented in order to fit the experimental data collected on MOS capacitors.

Figure 1 shows the ideal curve of the MOS capacitor mentioned above, where a significant discrepancy is observed, particularly in the shift of the two curves caused by the presence of fixed charges in the oxide near the oxide/semiconductor interface. Figure 2, in fact, depicts a C-V curve that includes the component related to the fixed charges we calculated, approximately $1 \cdot 10^{12}\,cm^{-2}$, which shifts the curve towards negative voltage values. Finally, the introduction of interface traps, whose profile is shown in Figure 3, causes a change in the slope of the C-V curve in Figure 4. To generate the trap profile, two distinct trap distributions were used and summed, taking into account the trends of the D_{it} tabulated in the literature [4,5]: an acceptor trap profile with an exponential distribution, a maximum concentration of $3 \cdot 10^{12}\,cm{-}2\,eV^{-1}$, starting from the conduction band energy level and decreasing exponentially with a sigma of 0.18; and a Gaussian profile centred 0.45 eV below the conduction band, with a maximum concentration of $1.5 \cdot 10^{11}\,cm^{-2}\,eV^{-1}$ and a sigma of 0.2.

Although this is a preliminary study on the calculation of interface traps, the development of a mathematical model capable of accurately predicting the final shape of the C-V curve of a MOSCap represents a fundamental step toward its application as a model for the channel region in a MOSFET. This approach will enable the separation of the contributions of individual capacitive components and a more in-depth investigation into the role these traps play in altering channel mobility.

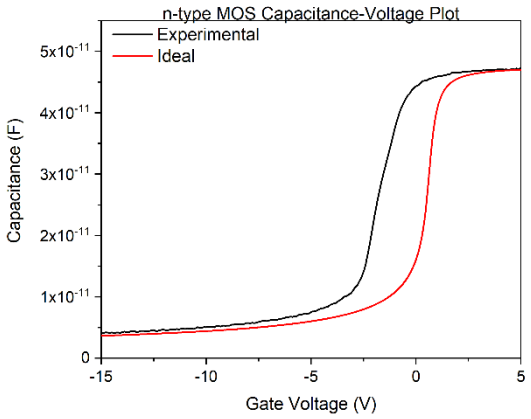

Figure 2: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve

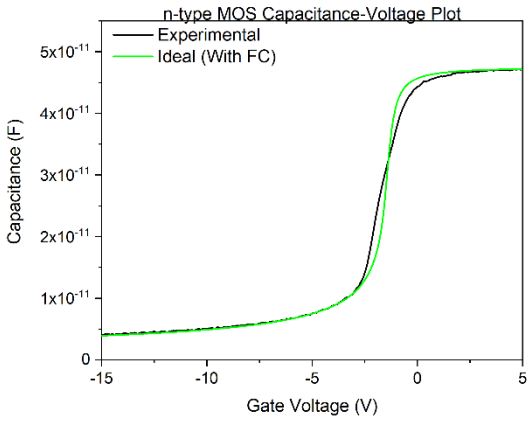

Figure 1: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve (FixedCharge were added)

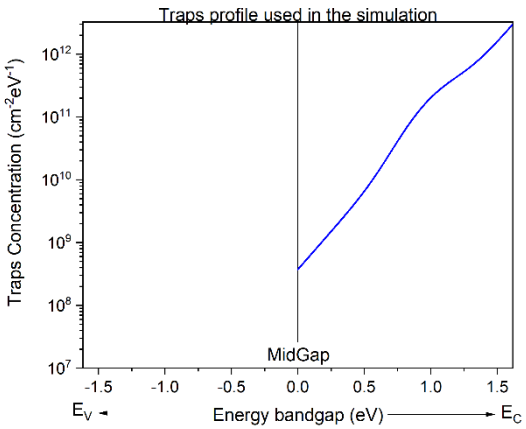

Figure 3: Interface traps used for the simulation of the final curve plotted in figure 4

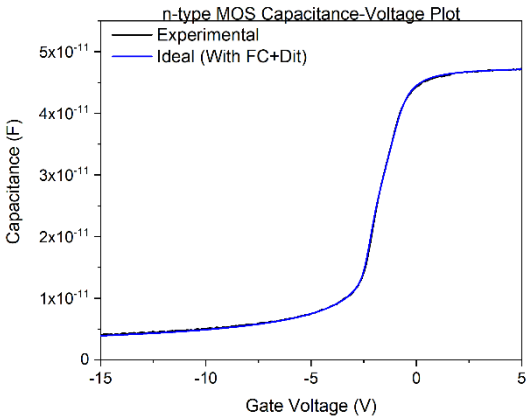

Figure 4: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve (FixedCharge and Dit were added)

References

[1] Tsunenobu Kimoto, 2016, "Bulk and epitaxial growth of silicon carbide", Progress in Crystal Growth and Characterization of Materials, Volume 62, Issue 2.

[2] Pantelides, S.T., Wang, S., Franceschetti, A., Buczko, R., Di Ventra, M., Rashkeev, S.N., Tsetseris, L., Evans, M.H., Batyrev, I.G., Feldman, L.C., Dhar, S., McDonald, K., Weller, R.A., Schrimpf, R.D., Fleetwood, D.M., Zhou, X.J., Williams, J.R., Tin, C.C., Chung, G.Y., Isaacs-Smith, T., Wang, S.R., Pennycook, S.J., Duscher, G., Van Benthem, K., Porter, L.M., 2006, "Si/SiO2 and SiC/SiO2 Interfaces for MOSFETs – Challenges and Advances", MSF.

[3] Fiorenza, P., Giannazzo, F., & Roccaforte, F., 2019, "Characterization of SiO2/4H-SiC interfaces in 4H-SiC MOSFETs: a review", Energies, 12(12), 2310.

[4] Potbhare, S., Goldsman, N., Pennington, G., Lelis, A., & McGarrity, J. M., 2006, "Numerical and experimental characterization of 4H-silicon carbide lateral metal-oxide-semiconductor field-effect transistor", *Journal of Applied Physics*, *100*(4).

[5] Maresca, L., Matacena, I., Riccio, M., Irace, A., Breglio, G., Daliento, S., 2020, "TCAD model calibration for the SiC/SiO 2 interface trap distribution of a planar SiC MOSFET", In *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)* (pp. 1-5), IEEE.