Enabling Ultra Low Temperature Hybrid Bonding for D2W Scaling

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Abstract:

Hybrid bonding is the next generation 3D integration technology that offers opportunities for extremely high interconnect densities (up to 1M IOs/mm^2 or more, [1]), significantly lower interconnect power [2] as well as improved thermal and power delivery performance [3, 4]. This can offer significant improvements in system performance and energy efficiency, especially for current and future AI and datacenter workloads. However, hybrid bonding offers several new challenges on cleanliness, dielectric and metal pad topography [5]. Additionally, several hybrid bonding schemes requires relatively high anneal temperatures to ensure good metal to metal bonding which can limit the capability of integrating temperature sensitive devices and potential mechanical impacts for complex die structures or larger chiplet sizes. To address these issues, we developed ultra-low temperature hybrid bonding (ULT-HB) technology targeting bonding temperatures <=200C. Several groups have been investigating copper grain engineering; as materials like nT-Cu and fine grain Cu has demonstrated higher expansion at lower temperatures (which can help reduce the CMP requirements), improved diffusivity, and are promising candidates for ultra-low temperature hybrid bonding [6-9]. Yet, engineered crystalline Cu is only part of the equation, for this technology to be fully viable within ultra-low temperature hybrid bonding all parts of the HB process need to be investigated, including surrounding dielectrics. In this talk, we will present on wafer-to-wafer and die-to-wafer compatible hybrid bonding using fine grain Cu. We will show wafer to wafer bonding results for 3 µm pitch at temperatures between 150 - 250 ^{o}C. Comparisons between types of Cu grain engineering vs. Std Cu, CMP slurry impact, pad recess impact, Cu grain stability, and discussion of current limitations and key drivers are shown.

Citations:

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