Localized sub-25nm Ruthenium and Rhodium Vertical Interconnect Access (VIA) Formation Implementing Airgaps

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This presentation focuses on the fabrication of localized sub-25nm ruthenium and rhodium vertical interconnect accesses implementing surrounding airgaps. The semiconductor industry has reached a point where, in principle, only a few options for highly specialized processes are possible for a particular manufacturing step. In recent years, the implementation of ruthenium and rhodium has become increasingly important due to its higher conductivity at nano meter scale. The subtractive approach has become the dominant process to manufacture vertical interconnects using these metals. [1] On the other hand, these metals are very expensive in their purest form and are only controlled by very few mining countries. As long as the electronic properties outweigh the high cost of the materials, the subtractive approach is going to be attractive. Our research focuses on the opposite of this approach: additive formation of vertical interconnects [2]. Metallic clusters (<0.5 nm) are generated by a spark discharge of 5 to 10 W. An inert forming gas flow (5% H_2 in N_2) transports the clusters onto a pre-patterned substrate, where the metal clusters deposit in a localized fashion. The funneling effect to guide the clusters into the patterns is controlled by the transport gas ions, which are in the clear majority within the process. [3] The gas ions charge up the insulating oxide layer and act as a pillow which deflects the metal clusters into a localized vertical interconnect access. The flux of material is self-alinging centered to the middle of the VIA and is free-standing without interaction to the VIA wall. [4] The resulting vertical interconnect is surrounded by an airgap. The size of the airgap can be controlled by the number concentration of surface charges which create the funnel. This number concentration is a function of the VIA aspect ratio and the spark discharge power. [2]

References

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