

Impact of Ti interlayer on the formation of Co silicides.

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In microelectronics, particularly in CMOS technology, metal silicides (TiSi₂, NiSi, and CoSi₂) have been widely used as contacts (i.e., to form source, drain, and gate contacts) [1]. Specifically, the CoSi₂-based contacts are still interesting for 65 nm technology despite the difficult nucleation of CoSi₂ in small dimensions [2]. Besides, the CoSi₂ phase in hetero-epitaxy offers low resistivity, better thermal stability, and low interface roughness, which are key parameters for small-dimension devices. Several studies have shown that adding an interlayer, such as Ti, Ta, Zr, Cr, V, and Mo, between Co and the Si substrate significantly boosts the growth of epitaxial CoSi₂ on Si [2,3]. Also, interlayers play a crucial role as a diffusion and reaction barrier for initial Co-Si reactions. However, the impacts also rely on the various experimental parameters like annealing ambient and temperature, layer thicknesses, etc [2,3]. Hence, understanding the effect of the Ti interlayer on the formation of CoSi₂ is important.

Therefore, in this work, we systematically investigated the impact of thin Ti interlayer on the formation of Co disilicides. After cleaning the Si₁₀₀ substrate (i.e., 300 mm), 3 nm and 5 nm Ti interlayers, 7.5 nm Co films, and a 10 nm TiN protective layer were prepared using the PVD technique. Numerous sample pieces (i.e., TiN/Co/Si (reference, without Ti), TiN/Co/3nm_Ti/Si, and TiN/Co/5nm_Ti/Si) were annealed using rapid thermal annealing (RTA) between 100 and 900°C with a temperature step of 20°C. Then, the X-ray diffraction (XRD) and the surface resistance (Rs) measurements were carried out at ambient conditions to understand the Ti interlayer impacts on the formation of Co silicides. The XRD results (**Fig. 1**) show that the presence of 3 nm and 5 nm Ti interlayer during the formation of Co silicides significantly modifies the formation temperatures and possibly the phase sequence (**Fig. 1b**). In particular, an additional phase called X is formed at low temperatures (around 300 °C). Mainly, the diffraction peak of the CoSi₂ phase is noticed between 530 and 630°C for 3 nm_Ti and between 550 and 610°C for 5 nm_Ti compared to the reference sample (observed up to 900°C). At temperatures higher than 660°C, diffraction peaks at $2\theta = 27.4^\circ$ and $2\theta = 39.3^\circ$ were noticed and attributed to the TiO_x and TiSi₂. Moreover, from 820 to 900°C, various diffraction peaks (i.e., $2\theta = 40.8^\circ$, $2\theta = 42.8^\circ$ and $2\theta = 45.0^\circ$) were observed. In **Fig. 2**, especially for the reference sample, the Rs behavior remains stable below 200°C then gradually increases up to 400°C, attributed to the successive formation of the Co₂Si and CoSi phases. Then, a plateau is noticed until a sharp decrease in Rs around 520°C, attributed to the formation of the CoSi₂ phase. However, the behavior is slightly different for Ti interlayer samples. In addition, a specific annealing temperature (600°C, 10 mins) was chosen to study the presence of heteroepitaxy of fully formed CoSi₂ phase, verified with XRD measurements (**Fig. 3**). The reference and Ti interlayer films (without TiN capping) show a diffraction peak at $2\theta = 33.7^\circ$, attributed to the CoSi₂ (200) phase in hetero-epitaxy, which is not observed for Ti films (with TiN). Also, TEM-EDX observations were carried out on TiN/Co/Si and TiN/Co/5nm_Ti/Si films after a Salicide process (RTA1@550°C 60 s/selective etching/RTA2@790°C 20 s) to confirm the hetero-epitaxy of the CoSi₂ layer obtained during the growth of Co silicides through Ti interlayer (**Fig. 4**). The TEM images show a CoSi₂ layer above the Si substrate, and the thicknesses vary between 22 & 29 nm (TiN/Co/Si) and 7.7 & 13 nm (TiN/Co/5nm_Ti/Si). These difference in thicknesses possibly comes from the weaker diffusion of Co through a Ti interlayer, which induces limited reaction during the Salicide process. Overall, this study is beneficial for understanding the Ti interlayer effect on the Co silicide formations and for the integration of contact formation in microelectronics.

References

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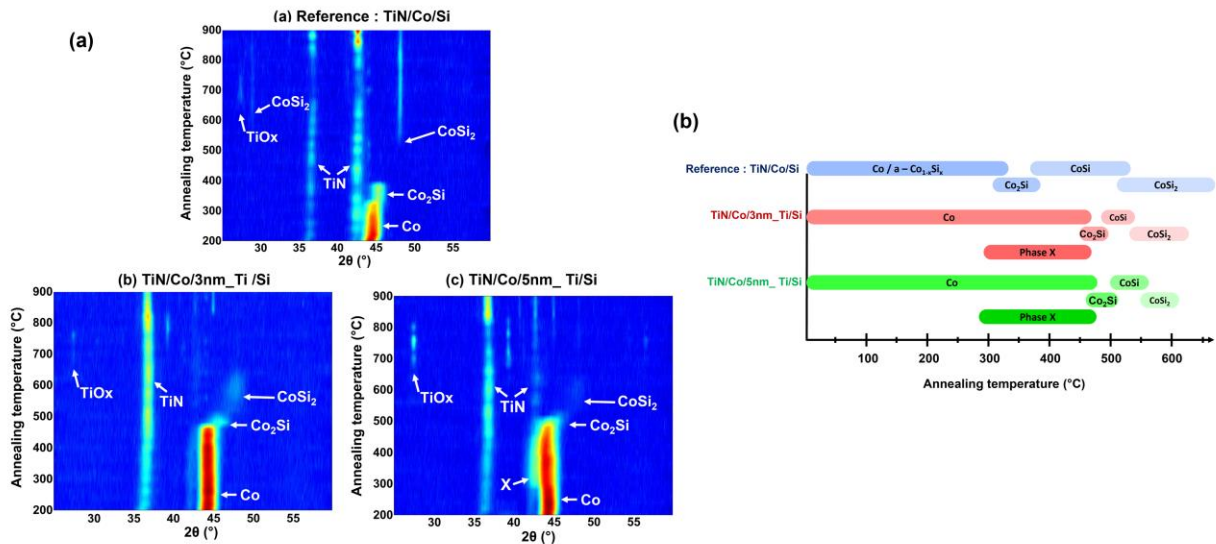


Fig. 1 (a) XRD patterns and (b) Schematic of phase formation, as a function of annealing temperatures for reference, and 3nm & 5nm Ti samples.

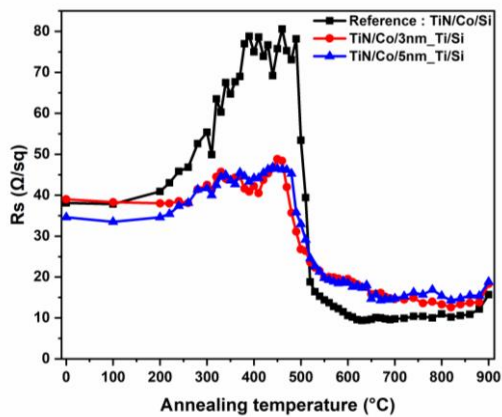


Fig. 2 Evolution of the Rs as a function of annealing temperatures for reference, and 3nm & 5nm Ti films.

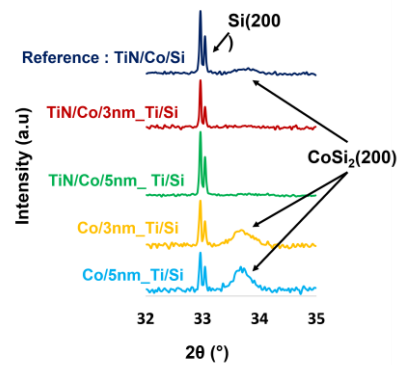


Fig. 3 XRD patterns for reference, and 3nm & 5nm Ti (with and without TiN) films annealed @ 600 °C/10 mins. .

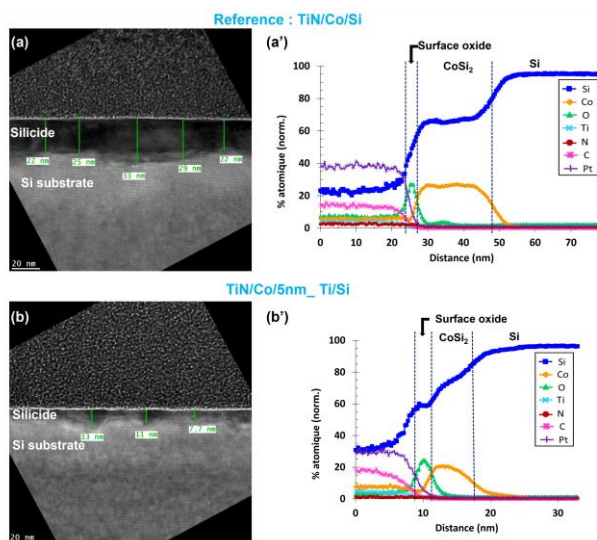


Fig. 4 TEM and EDX profile images after a Salicide process (550°C 60s/etching/790°C 20s) on samples (a and a') Reference TiN/Co/Si and (b and b') TiN/Co/5nm_Ti/Si films.