E-beam defectivity analysis of metal filled vias to determine yield of EUV lithography processes

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In this work we demonstrate a method to use metal fill process combined with voltage contrast SEM imaging to determine the yield of a via lithography process. In this method vias are formed with a CAR photo-resist using EUV lithography on both 0.33NA (NXE 3400) and 0.55NA (EXE 5000) and etched into a patterning stack containing a Ti base metal plate. In an ideal case, where both the lithography and etch are processed correctly, the via lands on the Ti base metal plate and a bright circular image is observed after metal fill. However, if defect occurs during these processes, the via may not land on the Ti base metal plate and a grey or black image is seen and a defect is identified. Using high NA (0.55NA) lithography CD-SEM images show a defect-free random vias pattern with a centre-to-centre (C2C) distance of 29.7nm.

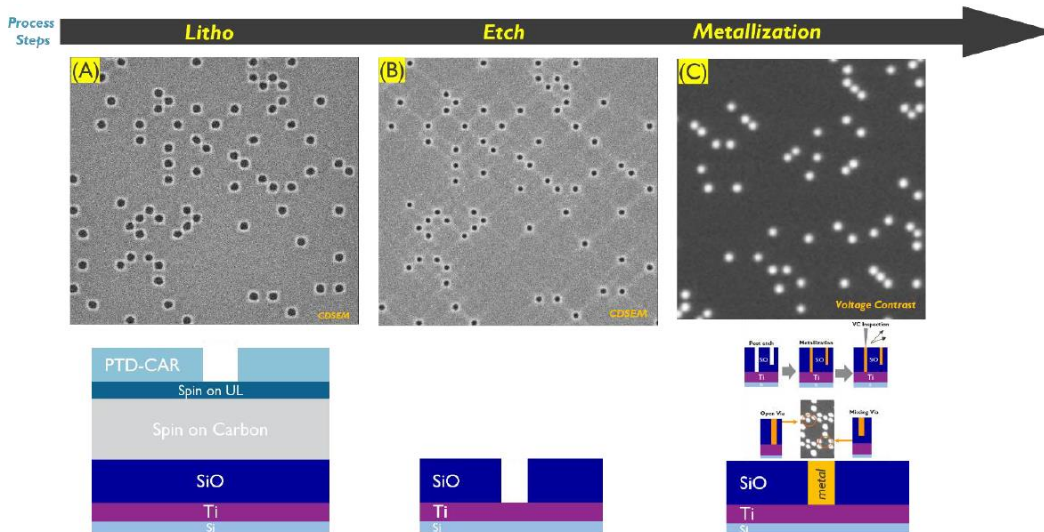

Figure 1: ***Baseline Process flow for random logic via***. (A) LNA EUV lithography and top-down CDSEM image. (B) Etch shrink showing defect free CD. (C) Voltage Contrast metrology principle and read out.

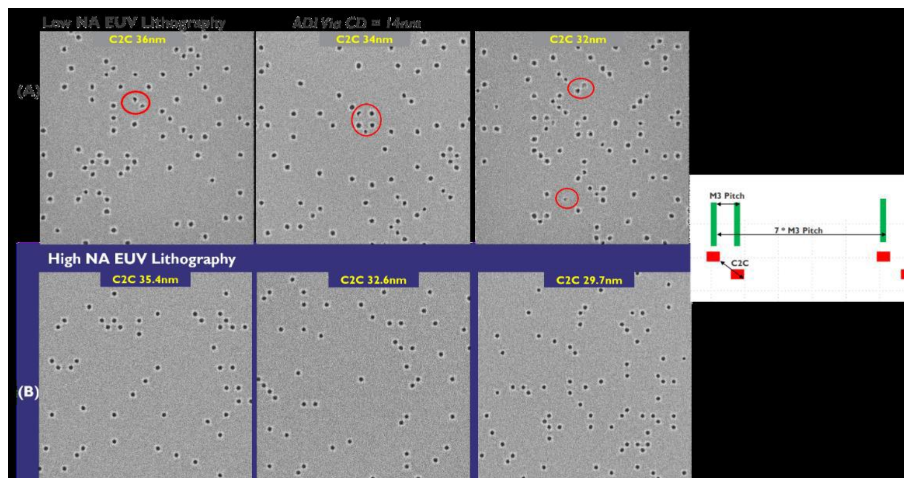

Figure 2: Comparison of Low NA EUV Lithography vs. High NA EUV Lithography. (A) At LNA, it is challenging to print defect-free via CD = 14nm and below. The red circles indicate the defects. (B) The bottom images are from High NA EUV lithography, showing zero defects even for smallest center-to-center distance of vias. The right image explains the alignment of the C2C distance of vias to the respective metal layers.

References

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