Challenges in Ru Damascene Integration for Future Interconnects

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Node-to-node scaling is reducing the transistor size and requires the interconnect pitch to follow to be able to connect the increased transistor density. Providing such tight pitch interconnects with conventional DD Cu structures is becoming more challenging below the 14nm critical dimension due to the intrinsic material properties of Cu. Here Ru has advantages as an alternative metal to Cu. Ru enables barrierless interconnects that have a lower resistance, better electromigration properties [1] and they can be used in direct metal processing.

Ru integrated in a semi-damascene offers [2] several benefits such as high aspect ratio lines, airgap incorporation to reduce intra-level capacitance and reduce RC delay [3], and the fact that it does not need a chemical mechanical polishing step (CMP) for the integration. However, moving towards Ru semi-damascene interconnect structures is a significant change in complexity and integration, while such schemes need damascene Ru lines as well to create multilevel interconnects.[4]

Therefore, this paper addresses the challenges for the dual damascene integration of Ru. We discuss the learning on the Ru fill in lines studied in 11 – 36 nm wide structures. More specifically, we address the difficulties in processing encountered resulting from high Ru melting temperature and the resistance of Ru to oxidation making the planarization by chemical mechanical polishing challenging.

References

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