3D-stacking technologies: remaining challenges of co-integration of thin Ni(Pt)Si film and $TiSi_x$ contacts.

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In CMOS (Complementary Metal Oxide Semiconductor) devices, for technology nodes below 65 nm, Ni-based silicide has been widely used to provide an ohmic contact to the active Si regions (such as gate, source, and drain) [1]. Numerous advantages have been highlighted compared to previous Salicide integration (known as Self-Aligned Silicide), such as diffusion-controlled growth, which results in a smoother silicide/silicon interface, and easier formation in narrow active lines. Moreover, the formation of Ni(Pt)Si involves low silicon consumption, which enabled its introduction for Fully Depleted Silicon on Insulator (i.e., FDSOI) technology for the 28 nm node [2]. However, one of the major drawbacks of Ni(Pt)Si films is their low stability at high temperatures, i.e., morphological degradation due to the agglomeration phenomenon [3–5]. Particularly, for FDSOI technologies, the current thickness of Ni(Pt)Si films is reduced to 11 ± 1 nm, resulting in thin films prone to agglomeration. At device scale, solid-state agglomeration, or dewetting degradations, induce severe yield loss due to the obtained electrical discontinuity, as previously published [6]. Various published works have reported several key factors that promote Ni(Pt)Si layer agglomeration, such as film thickness, grain size, and texture [3–5]. More recently, we demonstrated a clear improvement in terms of agglomeration sensitivity of ultra-thin Ni(Pt)Si films for a specific annealing scheme, including Dynamic Surface Annealing (DSA) instead of the classical Rapid Thermal Annealing (RTA) [7].

Nowadays, new advanced 3D technologies such as FinFETs (Fin-type Field Effect Transistor), CMOS Image Sensors (CIS), or new smart power technologies are moving away from Ni(Pt)Si silicides to Ti-based silicide contacts [8]. In this context, Ti/TiN bilayers, usually used as diffusion barriers inside W contacts, have been employed as reactive metal layers to form TiSi-based ohmic contacts [9,10]. New 3D-stacking imaging technologies, among others, deal with a dual-layer device, where an image sensor is built on top of an up-to-date CMOS device ([11], Figure 1). This results in the co-integration of ultra-thin Ni(Pt)Si thin films and TiSi-based contacts in the same integrated circuit. Therefore, improving the Ni(Pt)Si layer sensitivity to agglomeration and forming TiSi-ohmic contacts at low temperatures appear to be critical for the integration of new 3D-stacking technologies.

In this paper, after a complete overview of different 3D-stacking integrations, we will discuss the advanced processes involved in the formation of ultra-thin Ni(Pt)Si films, including surface preparation, annealing schemes, and pre-amorphization by implantation (PAI). We will also cover the processes widely used for TiSi-based contacts optimization, such as Nano-seconds Laser Annealing (NLA). Finally, we will present the latest progress and the remaining challenges for such integrations.

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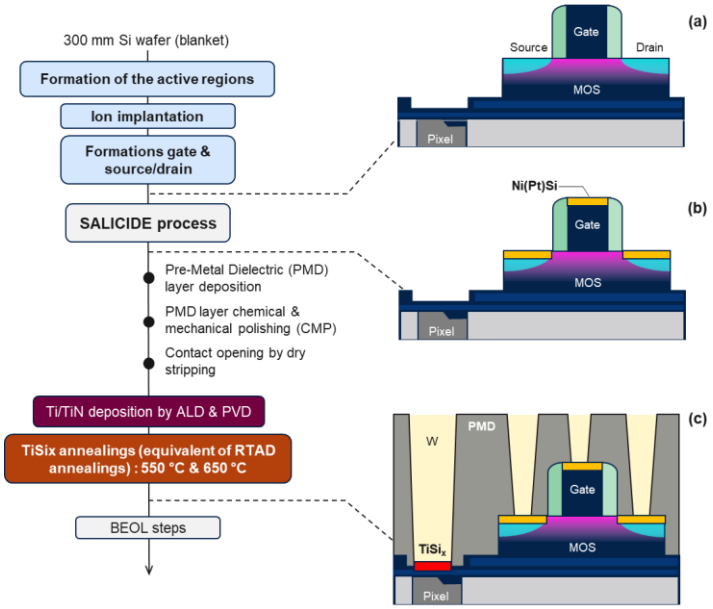

Figure 1. Description of a part of the process flow used to fabricate the integrated circuit involving the co-integration of Ni-silicide, Ni(Pt)Si and Ti-silicide, TiSiX presenting thermal budget incompatibility due to premature agglomeration of Ni(Pt)Si film during TiSix formation. Two type of annealings have been studied classical RTA (Rapid Thermal Annealing) and DSA (Direct Surface Annealing) to form Ni(Pt)Si thin films during SALICIDE process;

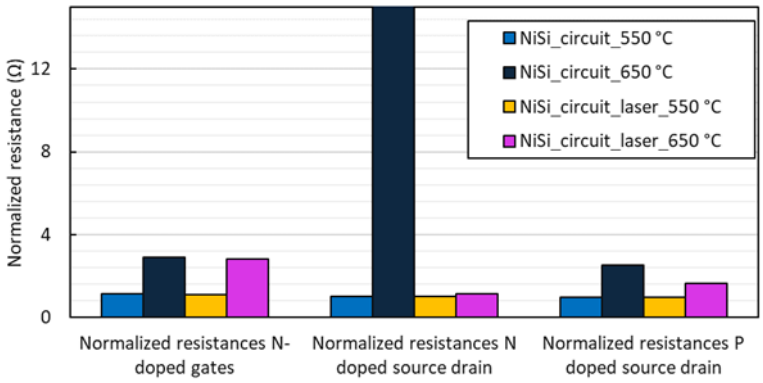

Figure 2. Normalized resistance, R (Ω), extracted from parametric tests on N-doped gates, source/drain, and P-doped source/drain for NiSi_circuit and NiSi_circuit_laser samples after $TiSi_x$ annealings at 550 and 650 °C.

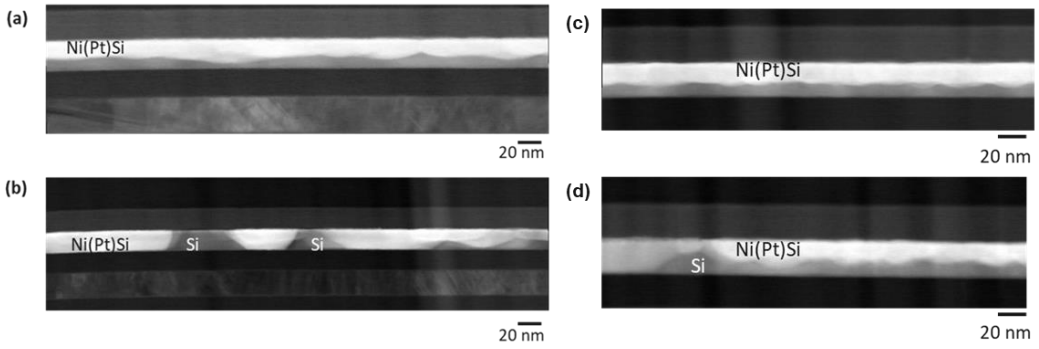

Figure 3 STEM cross-sections obtained for NiSi_circuit and for NiSi_circuit_laser samples for $TiSi_x$ annealings at (a,b) 550 and (c,d) 650 °C.