Vertically Scaled Gate-All-Around Transistors: From Advanced Nano-Contact Engineering to Device Development

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The continuous scaling of semiconductor devices has pushed conventional architectures to their physical limits, necessitating the development of novel transistor structures. Vertically scaled Gate-All-Around (GAA) transistors have emerged as a promising solution, offering superior electrostatic control, enhanced current drive, and high device density [1][2][3]. However, achieving high-performance and reliable device integration requires advanced engineering of nano-contacts and source/drain (S/D) interfaces [4].

This work presents a comprehensive investigation into the fabrication and optimization of nano-contacts for vertical GAA transistors. We explore the impact of channel nanostructured materials [5][6], contact silicide selection [7][8], and doping strategies on device performance [9], leveraging advanced characterization techniques to analyze dopant segregation [10] and silicidation effects at the nanoscale. Furthermore, we discuss process innovations that enable precise control over vertical channel formation, ensuring optimal electrical properties and minimal parasitic resistance.

By integrating experimental results with simulation insights, we highlight the critical role of nano-contact engineering in the development of high-efficiency, scalable vertical GAA transistors [11][12]. These advancements provide a pathway toward the next generation of ultra-scaled logic devices, enabling further transistor miniaturization while maintaining energy efficiency and performance in modern semiconductor technologies.

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