

# Electrical analysis of damascene patterned metal lines to evaluate patterning yield of EUV 0.33NA lithography

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A set of electrical test structures (serpentines and combs) are demonstrated to detect defects, line breaks and pinches, formed during lithography patterning. These structures were patterning using 0.33 NA EUV (NXE 3400) down as far as pitch 26nm and transferred using single damascene W metal fill. This method can demonstrate a combo yield (opens + shorts) of 99.7% for 1m long structures corresponding to a defect density of 12 defects/cm<sup>2</sup>. This method can be used as a platform to screen and test different aspects of lithography and patterning processes.

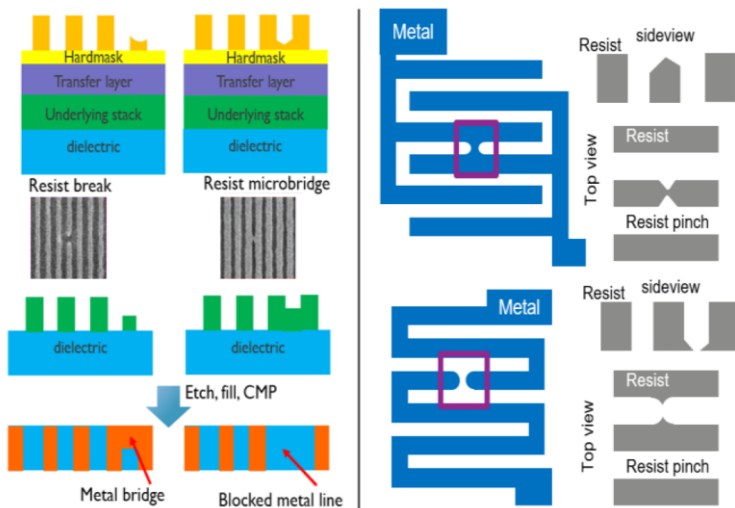


Fig. 1 Schematic representation of the different type or resist defects and its process transfer through full damascene process.

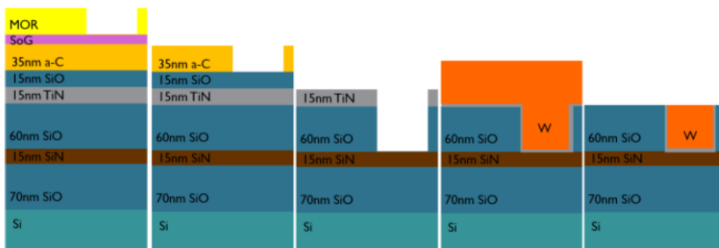


Fig. 2 Schematic representation of the fabrication process flow. From left to right: MOR resist exposure, pattern transfer into a-C hard mask, pattern transfer into final oxide layer, TiN hard mask wet strip and TiN liner and W CVD deposition, W CMP.

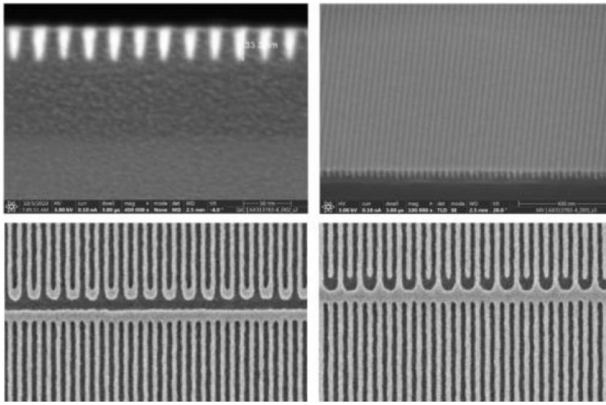


Fig. 3 Example cross-SEM pictures of fabricated devices after metallization and CMP (top) and top view CD-SEM inspection after etch inspection into TiN hard masks of meander and for structures.

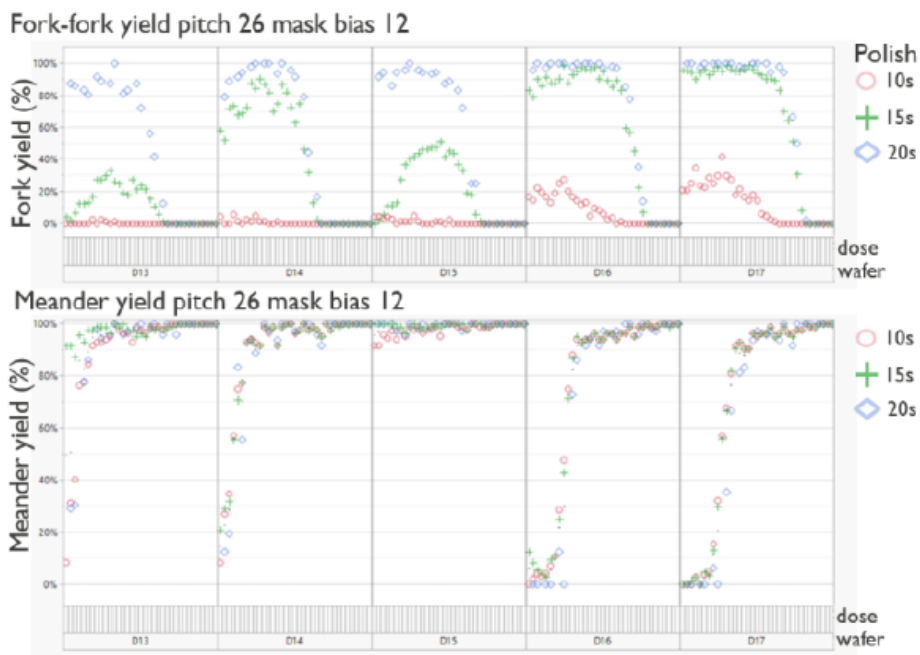


Fig. 4 Fork-fork (top) meander (bottom) yield for five different dose stripe wafers with various process conditions as function of CMP time for mask bias 12nm and one point per field electrical test measurements.

#### References

1. L. Tan, W. Gillijns, J. Lee, D. Xu, J. Kerkhove, V. Philipsen, R. Ki, " EUV low-n attenuated phase-shift mask on random logic Via single patterning at pitch 36nm", Proc. SPIE 12051, Optical and EUV Nanolithography 2022, 120510P (2022) <https://doi.org/10.1117/12.2614000>
2. Carballo, V.M. & Wachter, K. & Nafus, Kathleen & Feurprier, Y. & Thiam, Arame & Hsu, A. & Tabery, C. & Doise, J. & Schepper, P.. (2024). Patterning process and electrical yield optimization at the limits of single exposure EUV 0.33 NA: a pitch 26nm damascene process. 1-3. 10.1109/IITC61274.2024.10732293.

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