## Hybrid and Fusion Bonding to Enable Advanced Packaging

## Fumihiro INOUE

## YOKOHAMA National University, 79-5 Tokiwadai, Hodogaya, Yokohama, 240-8501, Japan

Direct bonding is emerging as a critical technology for advanced 3D architectures. Fusion bonding plays a pivotal role in enabling CFET and BSPDN structures in logic devices, as well as advanced 3D memory structures [1]. Similarly, hybrid bonding has become indispensable for meeting the stringent requirements of HBM, CIS, and 3D NAND development [2,3]. Despite its growing importance, the mechanisms underlying wafer bonding remain inadequately understood. Achieving ultimate distortion control is critical for precise overlay corrections during lithography. Bond wave behavior, the primary contributor to wafer bonding distortion, remains insufficiently explored. Plasma activation and surface wetting are thought to strongly influence bond wave speed, yet their surface-level interactions are poorly understood [4] (Fig. (a)). Furthermore, the lack of standardized bond strength measurement methods introduces significant variability in results [5] (Fig. (b)). In this paper, we will share our latest findings on the comprehensive study of wafer/die bonding mechanisms. These insights aim to support the evolution of future node 3D architectures.





## References

- 1. Yuh-Jier Mii, "Semiconductor Industry Outlook and New Technology Frontiers", 2024 IEEE International Electron Devices Meeting (IEDM)
- 2. Y. Kagawa et al., "Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding," 2016 IEEE International Electron Devices Meeting (IEDM),
- 3. M. Tagami, "CMOS Directly Bonded to Array (CBA) Technology for Future 3D Flash Memory," 2023 International Electron Devices Meeting (IEDM)
- 4. R. Sato et al., "Correlation between Pre-Bonding Surface and Bond Wave Speed" 2024 8th International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D)
- T. Iwata, et al., "Water stress corrosion at wafer bonding interface during bond strength evaluation." Materials Science in Semiconductor Processing 184, 108820 (2024)

\* Author e-mail: inoue-fumihiro-ty@ynu.ac.jp